Switching Converter Techniques for Energy Harvesting Applications

by

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This is to certify that I have examined the above MPhil thesis and have found that it is complete and satisfactory in all respects and that any and all revisions required by the thesis examination committee have been made.

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Switching Converter Techniques for Energy Harvesting Applications

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Abstract

Energy harvesting could provide a micro-sensor application with essentially a lifetime of power source, and there are many power management issues to be solved for efficient energy conversion. In this research, two design aspects of switch mode power converters targeted at employing an energy harvesting source were implemented. The first aspect is to start up a boost converter using a voltage close to the threshold voltages of MOS transistors, and converting a fluctuating input power to a regulated output voltage for sub-mA applications. The converter is called a threshold voltage startup (TVS) boost converter. The second aspect is store excess harvested power to a charge storage device such as a rechargeable battery or a super capacitor, to be retrieved when energy harvesting is periodically interrupted, such that the application could operate basically continuously. A single-inductor dual-input dual-output (SI DIDO) boost converter was developed to provide two regulated output voltages for the load and the energy storage device, and the energy harvesting source and the charge storage device are multiplexed to serve as the input. The TVS and SI DIDO boost converters were designed and fabricated using a 0.35μm CMOS process. Measurement confirmed that the TVS converter could start up with 0.65V that is midway between the threshold voltages of the NMOS and PMOS transistors and provided a regulated output voltage of 1.2V at 1mA with an input voltage that ranged from 0.2V to 0.9V. The SI DIDO converter could choose between two inputs and give two regulated output voltages, 1.2V and 2.4V. The 2.4V output was for the load, and the 1.2V was for the charge storage device.
Chapter 1

Introduction

1.1 Motivation

1.1.1 Use of Energy harvesting

Energy harvesting can be employed in many applications, and one of the applications is the wireless micro-sensor network [Calhoun 05] that consists of several to thousands of distributed nodes which sense and process data, and pass the result to end-users. This application is useful for military target tracking, industrial monitoring and home environmental control, to name a few. Since there are too many sensing nodes in the network, it is impossible to replace batteries for these nodes from time to time, and energy harvesting techniques with energy storage components could theoretically provide these nodes with a lifetime of power.

Another example of energy harvesting is for a person to wear an energy harvester [Paradiso 06] and collect energy to recharge the batteries of portable applications such as mobile phones and PDAs. Thanks to the energy harvester, sizes of batteries in those appliances could be reduced. The total weight of appliances plus energy harvesters does not increase significantly, but their lifetimes are extended. In fact, Seiko Kinetic wristwatches, smart tennis racquets, smart sports shoes [Cao 07] and Citizen Eco-drive watches [Citizen] are good examples of energy harvesting appliances.

1.1.2 Sources of Energy Harvesting

In the past decades, feature size of MOS transistors keep decreasing and computation power of an integrated circuit keep increasing, the number and variety of embedded digital electronics exploded, but with a relatively slow-improving battery technology [Amirtharajah 06]. With the advances in low voltage and low
power IC design techniques, even extensive analog and digital computation could be achieved in the micro-watt power range. This power range matches the power available from energy harvesting sources in the square or cubic centimeter range. These sources can be classified as mechanical, radiant, thermal and biochemical. Mechanical energy sources provide energy from various motions, for example, piezoelectric energy [Raghunathan 05] from human power during walking or other activities [Chapman 04] [Paradiso 06]. Radiant energy sources give energy from radiation sources, such as antennae and solar cells. Thermal harvesters generate energy by making use of the temperature difference at two locations, for example, thermocouple, and one of the biochemical energy sources is the fuel cell. Table 1.1 shows some harvesting technologies and their power densities [Raghunathan 05].

<table>
<thead>
<tr>
<th>Harvesting technology</th>
<th>Power density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solar cells (outdoors at noon)</td>
<td>15mW/cm²</td>
</tr>
<tr>
<td>Piezoelectric (shoe inserts)</td>
<td>330μW/cm³</td>
</tr>
<tr>
<td>Vibration (small microwave oven)</td>
<td>116μW/cm³</td>
</tr>
<tr>
<td>Thermoelectric (10°C gradient)</td>
<td>40μW/cm³</td>
</tr>
<tr>
<td>Acoustic noise (100dB)</td>
<td>960nW/cm³</td>
</tr>
</tbody>
</table>

Table 1.1: Different harvesting technologies with their power densities

1.1.3 Energy Storage in energy harvesting system

The output power levels of energy harvesting sources depend on the environment around them. Therefore, the energy harvested is unstable, fluctuating and even not available at times. Solar energy depends on the light intensity that varies dramatically with a 24-hour solar cycle and is affected by cloud coverage for outdoor applications [Amirtharajah 06]. Electricity generated from thermocouples also varies a lot as a person who wears it may travel from indoor to outdoor. In addition, different people have different activity paragons, and extracting thermal power is rather unpredictable.
Some energy harvesting applications are capable of adapting to a source that is fluctuating or even temporary not available, for example, the system in [Tsui 05] operates with a pipeline stage that does not depend on a global clock but only on the completion of the previous stage. However, many systems need to operate continuously. Thus, energy storage is needed to store the excess energy and provide energy to the system when the energy harvesting source is not available.

There are two common energy storage components: miniature rechargeable battery and super-capacitor [Raghunathan 05] [Smith 02]. Although both components have nonidealities common to regular batteries, such as self-discharge, round trip efficiency, decision of energy usage and storage in system [Raghunathan 05], using them in energy harvesting system can average out the power fluctuation generated from the energy harvester and provide a comparatively stable power source.

### 1.1.4 Needs of converters for energy harvesting application

Three output power profiles could be classified for energy harvesters. The first
power profile is as constant as a regular battery, but such a profile is unrealistic. The second power profile is fluctuating and the third intermittent, and could be regarded as ill-behaved. Even with an ill-behaved power profile, most systems still require a constant voltage supply, and the voltage converter can be a charge pump or a switching converter.

In this research, two techniques are proposed for switching converters in dealing with an ill-behaved power profile. The first technique is to jump start a boost converter even the power source provides a very low output voltage, close to the threshold voltage of MOS transistors. This technique is called Threshold Voltage Startup (TVS), and a TVS boost converter for sub-mA application is designed. The power source such as a solar cell may fluctuate but the regulated boost converter could provide a constant dc source.

The second technique deals with an intermittent power source, such as a rectified piezoelectric power from an energy harvester inside shoes [Cao 07]. The output voltage may stay fairly constant when the person is walking, but it may drop to zero when the person is sitting or standing. A Single-Inductor Dual-Input Dual-Output (SIDO) boost converter [Ma 01, Ki 01, Ma 03] is developed to provide two regulated output voltages for the load and an energy storage device, and the energy harvesting source and the energy storing device are multiplexed to serve as the input.
1.1.5 Comparison of power loss between different connections of batteries

![Fig.1.2: battery-array in series connection](image1) ![Fig.1.3: battery-array in parallel connection](image2)

All batteries in Fig. 1.2 and Fig. 1.3 are sourcing a voltage $V$ with an internal resistance $r$. In Figure 1.2, the batteries are connected in series and the equivalent internal resistance is $Nr$. In Figure 1.3, the batteries are connected in parallel and the equivalent internal resistance is $r/N$. The battery arrays are used to supply a power of $P$ to the load. For the battery-array in Fig. 1.2, the current is approximately

$$I = \frac{P}{NV}$$

and the power loss by the internal resistance of the battery-array is

$$P_{\text{loss-series}} = I^2Nr = \frac{1}{N} \frac{P^2r}{V^2}$$

For the battery-array in Fig. 1.3, the current is approximately

$$I' = \frac{P}{V}$$

and the power loss by the internal resistance of the battery-array is

$$P_{\text{loss-parallel}} = \frac{I'^2}{N}r = \frac{1}{N} \frac{P^2r}{V^2}$$

Hence, the power loss is the same.

Output voltage of connecting solar cell in parallel is 0.2V to 0.9V and boost converter is needed for a 1.2V regulated output.

Output voltage of connecting solar cells in series may be 0.4V to 1.8V or even higher, non-inverted flyback converter is needed rather than boost converter to give a 1.2V regulated output. In fact, large amount of chip area for power MOS is needed in flyback converter, so connecting cells in parallel is more chip area saved.
1.1.6 Different implementation of DIDO

![Diagram](image1)

**Fig.1.4:** Straightforward implementation of DIDO for piezoelectric application

Assume the output voltage of the piezoelectric cell is 1V, the nominal rechargeable battery output voltage is 1.2V, and the portable device needs a 2.4V supply. Straightforward implementation of a DIDO converter as shown in Fig. 1.4, that is, the power source uses one converter to supply power to the portable device, a second converter to charge up the rechargeable battery, and a third converter to supply power from the rechargeable battery to the portable device. The implementation needs three inductors and six MOS power transistors, and consumes much area on the printed circuit board (PCB). Fig. 1.5 shows a more practical implementation. The power source uses one converter to charge up the rechargeable battery, and a second converter to supply power from the rechargeable battery to the portable device. This implementation needs two inductors and four MOS power transistors. However, the obvious disadvantage is that the power from the power source has to pass through two converters before reaching the load, sacrificing the efficiency. Our proposed implementation of DIDO converter is shown in Fig. 1.6. It needs only one inductor and 5 MOS power transistors. This method reduces area on PCB without greatly sacrificing efficiency when compared with the previous case.
1.2 Research Goals and Contribution

New techniques are needed to overcome the difficulties of converting the fluctuating and intermittent power profiles of energy harvesters as mentioned in the previous sub-section.

For the fluctuating power source such as a solar cell, the supply voltage may vary widely depending on the light intensity and the load. We assume an application that requires a supply voltage higher than the highest voltage that could be provided by the solar cell, such as 1.2V or 2.4V, and a boost converter is needed. The main challenge is to start up the boost converter with a supply voltage close to the threshold voltage of the process, which is around 0.65V for a 0.35μm CMOS process, and remain functional even the supply voltage goes down to 200mV or so, or goes up to higher than 0.9V. The technique is called threshold voltage startup (TVS).

For the intermittent power source, the supply voltage could drop to zero at times. To deal with this problem, a single-inductor dual-input dual-output (SI DIDO) boost converter that operates in discontinuous conduction mode (DCM) is designed. When the power source is available, it provides energy to the load (the first output), as well as charging up an energy storing device (the second output), such as a rechargeable battery or a super-capacitor. When the power source is absent, the energy harvester (the first input) will be disconnected from the converter, and the energy storage device (the second input) will be multiplexed to serve as the supply voltage to the converter. Depending on the nature of the power source, the inductor may charge up the two outputs with different activation cycles (to be defined in Chapter 4.2.5).

The threshold startup boost converter is modified from a conventional PFM (pulse frequency modulation) converter, and the SI DIDO boost converter is modified from a conventional DIDO PWM (pulsewidth modulation) converter. To design an area-efficient power multiplexer (MUX) an on-chip 5X charge pump is
needed. Therefore, many theoretical and operational aspects of charge pump and switching converters such as PWM, PFM, DCM, and compensation are discussed.

The two converters are designed and fabricated using a 0.35\(\mu\)m CMOS process. Extensive simulation and measurement results will be presented to demonstrate the feasibility of all the design concepts.
Chapter 2
Threshold Voltage Startup Boost Converter for Sub-mA Applications

2.1 Overview of TVS Boost Converter

Customers always want an extended power cycle (the interval to change or recharge a battery) for portable equipments. Energy harvesting got increasing attention for long lasting power, especially for micro-power applications, and solar power is one of them. For clean power, fuel cell is a competitive candidate. However, the electrical behaviors of solar cell or fuel cell are quite different from regular batteries, and converters with special features are needed.

Research and development (R&D) is very active for medium to high power applications for fuel cells and solar cell arrays. In this research, we would like to focus on very low voltage and very low power applications. A fuel cell or a solar cell could provide a very low supply voltage, and startup of the converter is a major
challenge. The relatively high internal resistance of the solar or fuel cell adds to the difficulty of the design. At a very low power level, a high efficiency converter is difficult to be designed, as the consumption of the control circuit becomes comparable to the load.

The minimum startup voltage of a switching converter is a critical factor to determine how low the supply voltage could be such that the converter starts to work. For a CMOS process, the lowest voltages to turn on NMOS and PMOS transistors are their threshold voltages $V_{tn}$ and $|V_{tp}|$. The threshold voltage startup (TVS) boost converter, to be discussed next, requires a startup voltage that is midway between $V_{tn}$ and $|V_{tp}|$. The startup process employs an adaptive ring oscillator that has two voltages as its supply voltages, and the higher one dominates the operation. When the startup process is completed, that is, when the output voltage reaches 1.2V, a control signal will be generated and the converter enters a handover process. When the handover process is completed, the adaptive ring oscillator will be shut down to save power, and the boost converter then works in discontinuous conduction mode (DCM) with a variable frequency. The flow of operation is shown in Fig. 2.1.

![Fig.2.1: Operation flow of TVS boost converter](image)

After the TVS boost converter is started up, the supply voltage may drop to as low as 200mV and the converter remains functional. Therefore, the TVS technique is suitable for fuel and solar cell with a single cell.

The measurement results, to be presented in Chapter 3, show that the lowest
startup voltage of the TVS boost converter is 0.65V (threshold voltages of NMOS and PMOS for the employed 0.35μm CMOS process are 0.59V and 0.7V respectively), the operation input voltage range is 0.2V to 0.9V and the regulated output is 1.2V with a load of 0.1mA to 1mA. The maximum efficiency is 83%.
2.2 Development of the Threshold Voltage Startup Mechanism

2.2.1 Startup Mechanism of Boost Converters

The startup of a buck (step-down) switching converter poses no problem, but not for a boost converter. However, very few papers in the literature discussed the startup circuitry for boost converters.

![System diagram of startup of [Leung 05]](image1)

![System diagram of proposed startup](image2)

One startup mechanism of a boost converter was discussed in [Leung 05]. It made use of a conventional ring oscillator with one supply voltage. Therefore, the minimum startup voltage $V_{st(min)}$ has to be higher than the threshold voltages of the employed process to turn on and off the power transistors effectively. In fact, the converter used a 0.6$\mu$m CMOS process with $V_{ln} = |V_{tp}| = V_{th(ave)} = 0.85V$, and $V_{st(min)} = 1.18V_{ln} = 1V$. With 1V for startup, the unregulated output voltage thus achieved is $1.2V_{st(ave)} = 1.2V$. In [Leung 05], the power stage was driven by the output voltage $V_o$ directly to turn on the PMOS power transistor, and the output capacitor is charged to the input voltage prior to the startup process. This charge up time is proportional to
$V_o$, and is longer for a higher $V_o$.

In the following sections, we propose a startup scheme such that the boost converter could be started up with $V_{th(ave)}$, and the unregulated output voltage achieved is $1.85V_{th(ave)}$. The process we used is a 0.35μm process, with $V_{in} = 0.59V$, $|Vtp| = 0.7V$, hence, $V_{th(ave)}$ (and so is $V_{st(min)}$) = 0.65V. When the supply voltage $V_s$ is equal to $V_{th(ave)}$, the startup circuitry is activated and powered by both the input voltage $V_s$ and the output voltage $V_o$ of the boost converter. The built-in positive feedback mechanism helps boosting the output voltage up, such that $V_{th(ave)}$ is good enough for the startup process. During startup, $V_o$ is unregulated, but when $V_o$ reaches $1.85V_{th(ave)} = 1.2V$, the control will be handed over to the PFM controller to arrived at the regulated output voltage. The results are summarized in Table 2.1.

<table>
<thead>
<tr>
<th></th>
<th>Minimum startup input voltage – $V_{st(min)}$</th>
<th>Output voltage ($V_o$) with $V_{st(min)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Leung 05]</td>
<td>1.18 $V_{th(ave)}$</td>
<td>1.2 $V_{st(min)}$</td>
</tr>
<tr>
<td>TVS BC</td>
<td>$V_{th(ave)}$</td>
<td>1.85 $V_{st(min)}$</td>
</tr>
</tbody>
</table>

*Table 2.1: Comparison of existing startup mechanism with that of TVS BC*
2.2.2 Adaptive ring oscillator

The basic component of a startup circuit is the ring oscillator. A 5-stage ring oscillator is shown in Fig. 2.2. Each stage is an inverter, and a traditional inverter with a supply voltage of $V_1$ is shown in Fig. 2.3. Clearly, the swing of each stage is $V_1$ and Gnd. For achieving threshold voltage startup, a modified inverter with two supply voltages $V_1$ and $V_2$ is proposed (Fig. 2.4). Assume the input to the inverter $V_{in}$ is connected to ground ($V_{in}$ is low, or '0') such that $M_n$ is off, with $r_{p1}$ and $r_{p2}$ the on-resistance of $M_{p1}$ and $M_{p2}$ respectively (Fig. 2.5), the high output voltage $V_{oH}$ can be computed

$$\frac{V_2 - V_{oH}}{r_{p2}} = \frac{V_{oH} - V_1}{r_{p1}}$$

(2.1)

and

$$V_{oH} = \frac{r_{p1}V_1 + r_{p2}V_2}{r_{p1} + r_{p2}}$$

(2.2)

Thus, $V_{oH}$ is sandwiched between $V_2$ and $V_1$. Next, assume $V_2 > V_1$, if the ring oscillator of Fig. 2.2 is constructed by the 2-supply inverter in Fig. 2.4, the voltage swing of $V_{out}$ of the ring oscillator is then $(r_{p1}V_1+r_{p2}V_2)/(r_{p1}+r_{p2})$ to gnd. We label it the adaptive ring oscillator, and it has a higher voltage swing than the traditional inverter.
2.2.3 Open-loop boost converter with adaptive ring oscillator

Fig. 2.6 shows the case when the power stage of a boost converter is driven by the adaptive ring oscillator with open loop control. In our implementation, the last inverter of the ring oscillator is split into two inverters which could actually be combined together. Fig. 2.7 shows the scheme with the oscillator in transistor level. Note that all inverter outputs swing between $V_{oh}$ of eqn (2.2) and ground.
At the beginning of startup process of the boost converter, $V_o = 0V$, and $V_{o(ring)}$ strings between $V_{oh}$ and ground, and $V_{oh} < V_s$. The ring oscillator gives a duty ratio of 0.5, and $V_o$ is changed towards $V_s$ through the power PMOS $M_P$. When $V_o$ is higher than $V_s$, $V_{oh}$ is then higher than $V_s$, increasing the gate drive of the power MOS transistors $M_P$ and $M_N$, and decreasing their on resistance, and thus giving out a higher $V_{oh}$. Because of this positive feedback mechanism, $V_o$ is boosted up with an increasing rate.
2.2.4 Open loop boost converter with adaptive ring oscillator with cutoff signal

The startup circuit is not needed after the boost converter is properly regulated with a PFM controller, and the cutoff signal is denoted as \( V_c \).

![Diagram of 2-supply inverter with \( V_c \)](image)

Fig. 2.8: 2-supply inverter with \( V_c \)

![Block diagram of 2-supply inverter with \( V_c \)](image)

Fig. 2.9: Block diagram of 2-supply inverter with \( V_c \)

![Simplified circuit diagram of adaptive ring oscillator with second modified inverter](image)

Fig. 2.10: Simplified circuit diagram of adaptive ring oscillator with second modified inverter

Fig. 2.8 shows the insertion of the cutoff signal \( V_c \) into the 2-supply inverter, and Fig. 2.9 shows the block diagram representation. When \( V_c \) is connected to high potential, the inverter is disabled and the \( x_{\text{out}} \) node is disconnected from both supply voltages \( V_s \) and \( V_o \). Fig. 2.10 shows how the adaptive ring oscillator is built using the 2-supply inverters with \( V_c \). When \( V_c = "1" \), the reset switch \( M_{\text{reset}} \) is used to define the floating output \( x_{\text{out}} \) as ground, while the \( x_{\text{out}} \)'s driving \( M_P \) and \( M_N \) remains floating such that \( M_P \) and \( M_N \) could be controlled by the PFM controller.
2.3 Startup of TVS Boost Converter

2.3.1 Basic logic components

The TVS boost converter has two operation modes – the startup mode and the PFM mode. Therefore, logic components have to be designed to operate under different operation modes.

Fig. 2.11 and Fig. 2.12 show the NAND_vc2 and NOT_vc2 gates with 2 supply voltages and the cutoff signal $V_c$. When $V_c = "0"$, they work as normal NAND and NOT gates. Their $V_{oH}$'s are between $V_s$ and $V_o$. When $V_c = "1"$, their outputs are isolated from both $V_s$ and $V_o$. Both NAND_vc2 and NOT_vc2 are used in the startup period only.

Fig. 2.13 shows a NOT gate with only the pull up branch of $V_s$ controlled by $V_c$, and is labeled as the NOT_vc1 gate. When $V_c$ is connected to ground, it works as a normal NOT gate and the $V_{off}$ is between $V_s$ and $V_o$. When $V_c = "1"$, only the pull up branch of $V_s$ is isolated from the output and the NOT_vc1 works as a normal NOT gate with $V_{off} = V_o$. The NOT_vc1 gate is used in the buffer of the power stage, because the power transistors have to work all the time, whether the converter is in the startup mode or the PFM mode. When the output of the power stage is lower than 1.2V, the gate drives of the power transistors need both $V_s$ and $V_o$ as the power supply. When the output of the power stage reaches 1.2V, the startup process is completed and the $V_c$ signal is activated as high and turns off the pull up branches of
V_s, and the NOT_vc1 gates are then supplied by V_o only to maximize the gate drives of power transistors, and minimize the conduction loss of power transistors in PFM operation.

\[ \text{Fig.2.14: Circuit diagram of NOT}_\text{vc}_e \]

\[ \text{Fig.2.15: Circuit diagram of NOR}_\text{vc}_e \]

Fig. 2.14 and Fig. 2.15 show the NOT_vc_e gate and the NOR_vc_e gate. When \( V_c = "0" \), the pull down branches of both gates are disconnected from ground and put the output nodes in the high impedance state with disconnecting the pull up branches with Vdd. When \( V_c = "1" \), both gates are activated to function as proper NOT and NOR gates.

### 2.3.2 Functional blocks for the startup mechanism

Circuit blocks used in the startup mechanism are discussed in this sub-section.

\[ \text{Fig.2.16: Circuit diagram of startup circuit} \]

\[ \text{Fig.2.17: Circuit diagram of buffer of power mos} \]

All logic gates in Fig. 2.16 are NOT_vc2 and NAND_vc2 gates, because the startup circuit has to be isolated from the power stage completely after the power stage is started to save power.
The start_up_1 block in Fig. 2.16 is used to sense the states of both power transistors $M_P$ and $M_N$ in the power stage, and adds delay before passing the states to the deadtime_vc block in Fig. 2.16. The deadtime_vc block inserts deadtimes to the gate drives of $M_P$ and $M_N$ to avoid shoot-through current and thus speeds up the startup process. The NOT_vc2b gate is a NOT_vc2 gate with a larger size to drive the buffer of $M_P$ and $M_N$ in Fig. 2.17.

The NMOS transistors $M_{cf1}$ and $M_{cf2}$ are added to ensure that the startup circuit can be completely isolated from the buffer of $M_P$ and $M_N$. When $V_c = "0", M_{cf1}$ and $M_{cf2}$ are turned off and have no effect on both node 3 and node 5. When $V_c = "1", M_{cf1}$ and $M_{cf2}$ are turned on, pulling node 3 and node 5 to ground, and also the pull-down branches of NOT_vc2b, while the pull-up branches of NOT_vc2b are connected to $V_c = "1"$. Hence, the outputs of the NOT_vc2b gates (node 41 and node 61) are in a high impedance state, and do not affect the operation of boost converter after startup.

The power transistors $M_P$ and $M_N$ are driven by a series of NOT_vc1 gates with increasing sizes. These gates use the power supply $V_s$ and the output voltage $V_o$ in the startup process, but use only $V_o$ after startup (refer to Fig. 2.13).

### 2.3.3 Startup mechanism

The main idea of threshold voltage startup is elaborated next.

![Circuit diagram of startup mechanism](image)
The startup circuitry of Fig. 2.18a can be analyzed in the digital domain, although the output voltage levels are between $V_s$ and $V_o$. Assume the system is initially relaxed such that $V_s = V_o = 0V$, and all oscillations stop. Then $V_s$ increases. The ring oscillator has thirteen inverting stages of various sizes, and oscillation starts once $V_s$ is high enough to cause the outputs of the inverters to switch. As node p and node n switch, turning on and off $M_P$ and $M_N$, charge is being transferred to the output and $V_o$ starts to rise. The supply voltage to the startup circuit rises also, and so as the switching frequency. This positive feedback action causes $V_o$ to increase faster and faster and when $V_o = 1.2V$, $V_c$ will be activated to "1", terminating the startup process.

Fig. 2.19 shows the simulation result of node 3 and 5. When $V_c$ is changed from “0” to “1”, node 3 and 5 are discharged to 0V and put the NOT $vc2b$ gates in high
impedance state, isolating the startup circuit from the power stage. Simulation result also shows that the startup circuit can be activated with $V_s = 0.65V = (V_{tn} + |V_{tp}|)/2$. The startup circuitry is only 2% the size of the power transistors. The switching frequency prior to the termination of the startup process could be in the order of MHz. Due to process variations the total startup time can not be predicted accurately.

2.4 Analysis of TVS boost converter

2.4.1 Principle of operation of TVS boost converter

Fig.2.20: Block diagram of threshold voltage startup boost converter
Chapter 2 Threshold voltage startup boost converter for sub-mA application

Fig. 2.20 shows the block diagram of the TVS boost converter and Fig. 2.21 shows the startup mode, light load operation, heavy load operation, and startup after shutdown. Fig. 2.21 shows how \( V_o \) increases faster and faster during startup. When \( V_o \) reaches the high voltage limit \( V_H \), the startup process stops, and the V-control generator set \( V_c = "1" \) and the converter enters the handover mode to avoid \( V_o \) from overshooting. After the short period of handover, the converter operates in PFM mode.

The PFM controller can be separated into two parts. The power transistor \( M_N \) is controlled by the N Trigger, Current Sensor and Comparator, and the power transistor \( M_P \) is controlled by the Active Diode Control. When \( V_o \) drops and \( bV_o \) drops below
V_{ref,L}, M_N is turned on and the inductor current I_L ramps up. When I_L reaches I_{peak}, M_N is turned off, and I_L charges up the V_x node and M_P is turned on by the Active Diode Control, and I_L charges up V_o through M_P. The inductor current ramps down, and when it drops to zero, M_P is turned off by the Active Diode Control. With both M_P and M_N are turned off, the converter then enters the free-wheeling mode. The ringing suppression transistors M_{ip} and M_{in} are turned on by the M_L Controller until the next cycle begins.

Fig. 2.21 shows that when the load increases, the switching frequency of the converter also increases. If V_o drops below V_L suddenly, the converter changes from the PFM mode to the startup mode directly to charge up V_o, followed by the handover process and eventually comes back to the PFM mode. As the converter operates in the PFM mode that is a variant of the band-band control, no compensation network is needed.
2.4.2 Circuit implementation

2.4.2.1 Voltage divider for $V_o$ that gives $bV_o$

![Fig. 2.22: Circuit diagram of potential divider with diode connection of PMOS](image1)

![Fig. 2.23: Circuit diagram of potential divider with cutting PMOS off](image2)

The voltage control loop needs a resistor string to generate the scaled output voltage $bV_o$ for comparing with the reference voltage $V_{ref}$. The minimum current of the converter is designed to be 100μA, and if the loss due to the resistor string is 1%, then the resistors have to be in the order of 1MΩ, which will take up too much silicon area. However, if $b = 0.5$, then we must use two transistors in series to get the required voltage division (Fig. 2.22). The output voltage $V_o$ is designed to be 1.2V, which is smaller than $2 \times |V_{tp}|$, hence the two PMOS transistors $M_{d1}$ and $M_{d2}$ are working in the sub-threshold region. The current is designed to be 1.2nA, and the power consumption can be ignored.

The transistor string could be form as shown in Fig.2.23, but as both transistors are cut off, the current is 1.2pA, and may be too small to drive the input capacitance of 1.8fF of the Comparator and the V-Control Generator.
2.4.2.2 Deadtime_vc block

Deadtime for the power stage can be generated by the difference in pull down time between NAND gate and NOT gate. Fig. 2.24 shows that, when the input \( i \) changes from "0" to "1", node 4 changes from "1" to "0" before that of node \( p_1 \), both node 6 and node \( p_2 \) change from "0" to "1" and both node 3 and node 5 change from "1" to "0" with the delay which is generated from node 4 and node \( p_1 \). There is the same reason why the rising of node 3 is faster than that of node 5 when node \( i \) changes from "1" to "0".

---

![Simulation of output of Deadtime_vc](image-url)
Fig. 2.25: Simulation of switching frequency of $V_o$ of TVS BC with $V_s$ equals 0.65V in startup process.

Fig. 2.26: Simulation of Deadtime$_{vc}$ with $V_s = 0.65V$ and $V_o = 0.65V$ with 57kHz input.

Fig. 2.27: Simulation of Deadtime$_{vc}$ with $V_s = 0.65V$ and $V_o = 1.2V$ with 10MHz input.

Fig. 2.25 shows the simulation result of the TVS boost converter with a 0.65V supply, which is the lowest possible supply voltage for startup. When $V_o$ is boosted up to close to 0.65V, the switching frequency is 57kHz. When $V_o$ is close to 1.2V, the switching frequency is 7MHz. Therefore, the Deadtime$_{vc}$ block has to function well from 50kHz to 7MHz.

Fig. 2.26 shows the simulation result of various signals when $V_o = V_s = 0.65V$, with a switching frequency of 57kHz. The rising edge deadtime is 1.39$\mu$s, the falling edge deadtime is 1.35$\mu$s. The average deadtime is 1.37$\mu$s. Therefore, the percentage of deadtime per switching period is 7.8%.

Fig. 2.27 shows the case when $V_s = 0.65V$ and $V_o = 1.2V$ with a switching...
frequency of 10MHz. The rising edge deadtime is 6ns, the falling edge deadtime is 7ns. The average deadtime is 6.5ns. Therefore, the percentage of deadtime per switching period is 6.5%.

From the above result, it shows that the Deadtime_vc block generates a deadtime that is about 7% of the corresponding switching period. We note that the switching period depends on how fast the supply voltage charges up the gate capacitance of the next stage through the pull up branch and how fast the gate capacitance of the next stage can be discharged through the pull down branch of the previous stage. We also note that the deadtime depends on the difference of the discharge time between the NAND gate and the NOT gate, which depends on the discharge time of the gate capacitance of the next stage through the pull down branch of the previous stage. Therefore, both switching period and deadtime depend on the same factor, and deadtime over period can be kept at an approximately constant ratio.

The fact that the deadtime is proportional to the switching period allows the startup circuit to function properly over a wide range of supply voltage, as the deadtime would not occupy too much of a period to leave not enough time to charge up the inductor and deliver power to the output.
2.4.2.3 V-control generator (Vc_gen)

Fig.2.28: Circuit diagram of Vc_amp

Fig.2.29: Circuit diagram of Vc_gen

Fig.2.29 shows the Vc_gen block for generating the control signal Vc to start the handover process. During startup, Vo is initially lower than Vs, and Vc is 0V. M7 of Vc_amp in Fig.2.28 is turned on by Vc. Therefore, the output nodes of the Vc_amp's swing between Vo and Vs. The scaled output voltage bVo is smaller than the predefined low threshold voltage VL, and Vc is kept at "0". When bVo increases to be between VH and VL, the inputs of the SR latch s_n and r_n are both high, and Vc remains as "0". When bVo is larger than the high threshold voltage VH, Vc is switched to "1", which is the same as Vo, and the handover process begins. After the handover process, bVo decreases and stay between VH and VL, and Vc remains as "1". The converter eventually enters the PFM mode. Note that when Vc = "1" = Vo, the startup circuitry will be shut off, including the paths from Vs to Vc_amp's to save power.
2.4.2.4 Handover process

![Circuit diagram of handover trigger](image)

**Fig.2.30:** Circuit diagram of handover trigger

![Truth table of components in handover trigger](image)

**Fig.2.31:** Truth table of components in handover trigger

![Simulation of TVSBC with (solid line) and without (dotted line) handover circuit](image)

**Fig.2.32:** Simulation of TVSBC with (solid line) and without (dotted line) handover circuit

The startup process of the TVS boost converter is an open loop process. When the startup mode is changed to the PFM mode, the value of the inductor current is unknown, and the PFM controller may not be fast enough to suppress potential output overshooting. Therefore, we need to determine the value of the inductor current right after the startup process. The simplest method to avoid output overshoot
is to turn off both power transistors $M_P$ and $M_N$, but turn on the free-wheeling switches $M_{ip}$ and $M_{in}$ to consume all the energy in the inductor first before starting the PFM control.

The handover process starts when $V_c$ changes from “0” to “1”. Fig. 2.30 shows the handover trigger. Node $s$ is connected to $V_c$, and node $r$ is connected to an internal node (node 2) of the Active_Diode_Control.

Node $s$ and node 1 are in opposite states, and so do node $r$ and node 11. Only an instantaneous change from "0" to "1" on node $s$ or node $r$ can give two instantaneous 0’s on both inputs of the respective NAND gate, and a "0" can be generated on node s2 or node r2 to control the state of node out1.

When the converter is in the startup mode, $V_c = 0V$, node out1 is forced to “1” by $M_{cf1}$, node out is “1”, and both $M_{cfn1}$ and $M_{cfn2}$ are cut off. When the startup process is finished, $V_c$ changes from “0” to “1”, node s2 gives a pulse of "0" to the NAND gate which is connected to it, and node out1 is pulled to “0” (Fig.2.31), and $M_{cfn1}$ and $M_{cfn2}$ are turned on by node out. Node 611 and 41 are connected to N part trigger and the buffer of $M_P$ respectively. Both node 611 and 41 is pulled to “0” and turn both $M_P$ and $M_N$ off. At the same time, the freewheel switches are turned on, dissipating the energy of the inductor. Therefore, overshoot of $V_o$ can be avoided.

When the inductor current falls to a prescribed value, the node voltage $V_x$ of the power stage decreases, node 2 of active_diode_control, which is node $r$ in the handover circuit, changes from “0” to “1”. Node r2 gives a pulse of "0" to the connected NAND gate, node out1 changes to “1” and node out changes to “0”, $M_{cfn1}$ and $M_{cfn2}$ are cut off. Node 611 and 41 are isolated from N-control trigger and the buffer of $M_P$. The handover circuit is then isolated from the rest of the circuit.

Fig.2.32 shows the simulation result of $V_o$ and the inductor current with and without the handover circuit. When the handover trigger is set to 1.2V, the highest $V_o$
with handover circuit is 1.2576V, while the highest $V_o$ without the handover circuit is 1.425V. Therefore, the handover circuit can prevent large output overshoot.

Even when $V_c$ changes from “1” back to “0”, it cannot change the state of node s2, and $V_c = “0”$ disables the handover circuit by cutting both $M_{cfn1}$ and $M_{cfn2}$ off. In addition, when node r changes from “1” to “0”, the handover circuit keeps its disabled state. Therefore, the handover circuit has no response when $V_c$ changes from “1” to “0”, and the PFM mode returns to the startup mode directly when $V_o$ drops suddenly.

The main purpose of $M_{cf}$ is to make sure that node out is equal to “0” to disable the handover circuit during the startup process. Therefore, the handover circuit is disabled when the converter is either in the startup or the PFM mode.
2.4.2.5 N-control part in PFM control

Fig.2.33: Circuit diagram of current source

Fig.2.34: Circuit diagram of comparator

Fig.2.35: Circuit diagram of current sensor

Fig.2.33 shows the self-biased current source which is used to provide the bias current of the control circuit. The transistor \( M_b \) is used to prevent the stable condition with no current flow. Consider the case when all \( M_1 \) to \( M_5 \) are off. If \( V_o \) is higher than \( V_{tn} \), \( M_b \) then conducts, pumping current into \( M_5 \) and turns on \( M_4 \), which sinks current from \( M_1 \) and turns on \( M_2 \), and the current source starts to work.

The Comparator block shown in Fig.2.34 is used to compare \( V_{ref\_L} \) with \( bV_o \) that are \( V_i^- \) and \( V_i^+ \) respectively. The output of the comparator is connected to nodes of the N part trigger. When \( bV_o \) is lower than \( V_{ref\_L} \), node out give a falling-edge signal to the N part trigger and \( M_N \) is turned on. The biasing transistor \( M_{b1} \) is biased by \( V_c \).

When \( V_c \) is 0V, the converter is in the startup mode, and no comparison between \( V_{ref\_L} \) and \( bV_o \) is needed. When \( V_c = V_o \), the comparator is activated. Using \( V_c \) as a biasing voltage reduces power consumption by cutting off the comparator that is not
used in the startup process.

Fig. 2.35 shows the current sensor used to sense the inductor current when \( M_N \) is turned on. The current sensor is biased by the current source. Node \( \text{in} \) is connected to \( V_x \) of the converter to sense the inductor current. \( M_1 \) and \( M_2 \) provide the same current to \( R_b \) and \( M_N \) via node 4 and node \( \text{in} \) respectively. The voltage across \( R_b \) and \( M_N \) are:

\[
V_{rb} = I_D \cdot R_b
\]

\[
V_{MN} = (I_D + I_L) \cdot R_{on} \approx I_L \cdot R_{on}
\]

where \( I_D \) is the drain current of \( M_1 \) or \( M_2 \), \( I_L \) is inductor current, \( R_{on} \) is on-resistance of \( M_N \) and \( I_D \) is much smaller than \( I_L \).

Assuming \( I_D \) and \( R_{on} \) are fixed. Because \( I_D \) is fixed by the current source and \( R_{on} \) is nearly fixed by the driving voltage of gate \( M_N \), therefore, \( V_{rb} \) and \( V_{MN} \) can be controlled by the value of \( R_b \) and \( I_L \) respectively. When \( M_N \) is turned on and \( I_L \) increases from zero such that \( V_{MN} \) is just larger than the pre-set \( V_{rb} \), node 2 of the current sensor rises up and node out gives the falling edge signal to the N-trigger to turn off \( M_N \).

A large peak inductor current cause a large conduction loss by \( M_N \) at the peak current and hurts the efficiency. Therefore, the best is to set the maximum peak inductor current such that at the minimum input voltage with the maximum load current, the converter is operating at the boundary between DCM (discontinuous conduction mode) and CCM (continuous conduction mode). Finally, the peak inductor current is set to around 42mA.

When \( M_N \) is turned on and the inductor is charging with the supply voltage, the inductor current is

\[
I_L = \frac{V_S}{L} \cdot t
\]

We design \( I_{L\text{max}} \) to be 42mA. Now, \( V_S \) ranges from 0.2V to 0.9V and \( L \) is 4.7\( \mu \)H, so the charging time of the inductor current \( t \) is between
0.99μs to 0.22μs. Therefore, the current sensor has to be fast enough. Since node in is connected to \( V_x \) of the power stage, and node 2 follows node in with a delay time of the inverter. Therefore, the change of \( V_x \) propagates to the next circuit block within two delay times of the inverter via node out.

For the converter, the maximum inductor current is set as 42mA and the minimum output current is 0.1mA. If we use a conventional current sensing NMOS transistor \( M_Y \) to sense \( M_N \) (shown as \( M_X \) in Fig. 2.36) and use \( R_s \) to convert the sensed current into \( V_{\text{sen}} \), the ratio between \( M_Y \) and \( M_X \) have to be 1 to 20000 for a 5% power consumption when \( I_{\text{load}} \) is 0.1mA. The large ratio makes the sensing accuracy very poor. The proposed current sensor is much more power-saving, and the accuracy could be improved if \( R_b \) is replaced by a matched transistor.

When \( V_c = 0\text{V} \), \( M_{cf} \) and \( M_a \) are turned on and off respectively in Fig. 2.35, and \( M_5 \) is turned off. The paths from \( V_o \) and ground to node out are both cut. Therefore, node out is in the high impedance state, and the circuit that is cascaded to the current sensor would not be affected when the converter is operating in startup mode. When \( V_c = V_o \) after the startup process, \( M_{cf} \) and \( M_a \) are turned off and on respectively, and node out is controlled by node 2 and act as a normal inverter.
Fig. 2.37: Circuit diagram of N-trigger

Fig. 2.38: Truth table of component in N-trigger

Fig. 2.37 shows the N-trigger block. The output of the comparator in Fig. 2.34 is connected to node s of this block and the output of the current sensor in Fig. 2.35 is connected to node r of this block. When the converter is in the startup mode, \( V_c \) is 0V, and all the NOR\(_{vc_e}\) and NOT\(_{vc_e}\) gates are disabled. Moreover, \( V_c \) turns Mcf on, which is used to cut off the pull up branch of the NOR\(_{vc_e}\) gate. This action makes sure that node out of NOR\(_{vc_e}\) is in the high impedance state, so node out would not affect the startup process.

When \( V_c = V_o \) after the startup process, all the NOR\(_{vc_e}\) and NOT\(_{vc_e}\) gates are enabled and work as normal NOR and NOT gate respectively. Fig. 2.37 shows that node s and node r are in opposite logic states in the steady state respectively. Therefore, node s2 or node r2 is in logic 0 in the steady state according to Fig. 2.38, and node out1 in Fig. 2.37 maintains its previous stage. Only instantaneous charging from 1 to 0 on node s or node r can give two instantaneous 0’s on both inputs of the NOR\(_{vc_e}\) gate, and a pulsing 1 can be generated on node s2 or node r2 to control the state of node out1.

\( M_{d1} \) and \( M_{d2} \) in Fig. 2.37 act as MOS capacitors to introduce RC delay to
lengthen the duration of the above pulsing 1 signal, making sure that it is long enough to trigger the state of node out1 in the N-trigger block correctly, but the propagation delay from node out1 to the buffer of the power transistor is not affected. The pulsewidth of the pulsing 1 has to be longer than the propagation delay of the trigger in Fig. 2.38 to make sure that the correct signal is passed out by the N-trigger block. However, the duration of it has to be shorter than the charging time of the inductor current to make sure that the set and reset signal from the comparator and the current sensor do not interfere with each other.

When the scaled output bVo of the converter is smaller than Vref_L, the output of the comparator in Fig. 2.34 pulls node s of N-trigger down and generates a pulsing 1 on node s2, and node out1 is set to 1. Node out of the N-trigger block is set to 0 and turns MN on via the inverted power buffer in Fig. 2.17. When the inductor current reaches Ipeak, the output of the current sensor pulls node r of N-trigger down and generates a pulsing 1 on node r2 and node out1 is set to 0. Node out of N-trigger is set to 1 and turns MN off via the inverted power buffer. In addition, most of the time, node s2 and node r2 stay as logic 0, and node out1 maintains its previous stage.

**2.4.2.6 P-control part in PFM control**

![Circuit diagram of active diode core 1](image1)

![Circuit diagram of active diode core 2](image2)

In simplifying the design of the converter, there is no control block to monitor both MP and MN. Therefore, MP is controlled alone by the zero inductor current sensing circuit. The simplest method to control MP is to build a control circuit similar
to a diode that is controlled by $V_c$.

Fig. 2.39 shows the active diode core 1 (AD1) modified from [Lam 06] and [Man 06], and is biased by node c4 of the current source. Node out is connected to the input of the power buffer in Fig. 2.17.

When the converter is in the startup process, $V_c = 0V$, putting AD1 in the high impedance state with turning $M_{cf}$ on and $M_a$ off. Therefore, $M_a$ and $M_5$ are turned off and do not affect the startup circuits in Fig. 2.16.

When the converter changes to the handover mode, $V_c = V_o$, and node out of AD1 is controlled by node 2 with $M_{cf}$ turned off and $M_a$ turned on. Therefore, $M_a$ and $M_5$ are turned on, and node out is an output of a dynamic logic which is biased by $M_6$ and the logic input is node 2. Dynamic logic is used on the output state of AD1 to speed up the signal propagation from $V_x$ to the buffer of the power transistor.

At the end of the handover mode, the inductor current falls to close to zero, and $V_x$ is smaller than $V_o$, pulling node 1 down and increases the $V_{sg}$ of $M_2$. Therefore, node 2 of AD1 gives a rising edge signal to node r of the handover trigger in Fig. 2.24, which terminates the handover process and the converter then operates in the PFM mode.

Consider the converter to operate in PFM mode. When the inductor current is larger than zero and $M_N$ is turned off, the inductor current is forced to flow to node $V_x$, charging the parasitic capacitor and $V_x$ rises. When $V_x$ is higher than $V_o$, node 1 is pulled up by $V_x$ and decreases the $V_{sg}$ of $M_2$, potential of node 2 decreases and that of node out increases, turning on $M_P$. The inductor current charges the output capacitor until it is zero, and the current starts to flow back from node $V_o$ to $V_x$. Therefore, $V_x$ is lower than $V_o$, and $V_x$ pulls the potential of node 1 down and increases $V_{sg}$ of $M_2$, the potential of node 2 is pulled up and that of node out is pulled down and turns off $M_P$. 38
In the PFM mode, when node 2 is pulled up, it gives a termination signal to the handover trigger, and $M_P$ is turned off, and the normal operation of PFM does not affected. When node 2 is pulled down, it does not affect the previous state of the handover trigger and $M_P$ is turned on. Therefore, node 2 does not affect the operation of PFM.

The structure of AD1 is an unbalance design. When $V_{sg}$ of $M_2$ is increased by pulling down node $V_x$, node 2 is pulled up by the current draw from $M_2$. When $V_{sg}$ of $M_2$ is decreased by pulling up node $V_x$, node 2 is pulled down by the current sink from $M_4$. The current drawn from $V_o$ to node 2 via $M_2$ depends on $V_{sg}$ of $M_2$ which can be quite large. However, the current sink at node 2 by $M_4$ depends on the bias current only, and this current is small to keep the static current consumption of AD1 low. Therefore, the pull up time of node 2 is faster than its pull down time, and the response of AD1 to turn $M_P$ off and on are about 12ns and 22ns respectively, as shown in Fig.2.41.

Fig. 2.40 shows the active diode core 2 (AD2), which is modified from AD1. In AD1, node $V_x$ is used to control the gate of $M_2$, which is used to control node 2. Therefore, change of node $V_x$ does not control node 2 directly in AD1. For AD2, $V_o$ and $V_x$ are interchanged. Node $V_x$ controls node 21 that controls node 2 in AD2 directly, and gate of $M_5$ is controlled by node 2 which is the output of the inverter that has larger driving force compared with node 2 in AD1. This design can speed up the propagation time from the active diode core to the circuit cascaded to it. Therefore, the response of AD2 is fast enough that no dynamic logic output state is needed, and static power consumption is less than that of AD1.
Fig. 2.41: Simulation of comparison of propagation delay between AD1 and AD2

Fig. 2.42: Simulation of TVS BC efficiency comparison between AD1 and AD2

Fig. 2.41 shows that when $V_x$ is larger than $V_o$ and $M_P$ is turned on, the response of AD2 is faster than that of AD1. When $V_x$ is smaller than $V_o$, $M_P$ is turned off, the response of AD2 is slower than AD1. However, no matter AD2 has faster or slower response compared with that of AD1, the difference are only around 3ns, and AD2 save static power compared to AD1. Therefore, the converter with AD2 has higher efficiency compared to AD1 as shown in Fig. 2.42.
2.4.2.7 \( M_L \) controller

Fig. 2.43: Circuit diagram of \( M_L \) controller

Fig. 2.44: Circuit diagram of ringing suppression circuit

Node a and node b of the \( M_L \) controller in Fig. 2.43 are connected to node p and 63 of the buffer of power mos in Fig. 2.17 respectively.

During startup, \( V_c = 0V \), \( M_5 \) and \( M_8 \) are turned off and on respectively, the NAND gate with input a and input b is disabled, node out\_n is pulled down by \( M_8 \) and node out\_p is pulled up by node out\_n. Ringing suppression switches \( M_{in} \) and \( M_{ip} \) are cut off.

After startup, \( V_c = V_o \), \( M_5 \) and \( M_8 \) are turned on and off respectively, the NAND gate with input a and input b is enabled and node out\_p is directly controlled by node out\_n rather than \( M_8 \). When both \( M_P \) and \( M_N \) are turned off, node out\_n and node out\_p are pulled up and down respectively, switches \( M_{in} \) and \( M_{ip} \) are both turned on, shorting the inductor that suppresses the ringing due to the inductor \( L \) and the parasitic capacitor \( C_L \) [Ma 03]. The transmission gate formed by \( M_{in} \) and \( M_{ip} \) is more effective than by \( M_{in} \) or \( M_{ip} \) alone.
Chapter 3

Measurement of TVS Boost Converter

The threshold voltage startup (TVS) boost converter was implemented in AMS 0.35μm CMOS process and the chip photo is shown in Fig. 3.0. The dimension is 675μm x 615μm.

In this chapter, the measurement results of the TVS boost converter are shown to verify its functionality and performance.

Fig. 3.0: Die-photo of TVS boost converter

Fig. 3.1 shows the startup response of the converter with $V_s = 0.65V$, which is
midway between $V_{tn} = 0.59V$ and $|V_{tp}| = 0.72V$.

Fig.3.1: Startup response of TVS boost converter

Fig.3.2: Vs=0.9V, 1mA loading  
Fig.3.3: Vs=0.9V, 0.1mA loading

Fig.3.4: Vs=0.2V, 1mA loading  
Fig.3.5: Vs=0.2V, 0.1mA loading

Channel 1: Vo with AC coupling  
Channel 2: Inductor current with DC Coupling  
Channel 3: Vx with DC coupling

Fig. 3.2 to Fig. 3.5 show the steady state response of the four extreme cases of operation. They are minimum or maximum supply voltage with minimum or
maximum current loading. The inductor current is too small to be measured by current probe (TCP A300, with resolution of 1A/1V with oscilloscope), hence, it is measured by the voltage drop across a 1Ω resistor in series using oscilloscope TPS 2024. The measured inductor current is very noisy, but the converter is actually operating in good DCM mode as shown by the trace of \( V_x \). When the inductor current is zero, \( V_x \) is equal to \( V_s \) rather than ringing, showing that the converter is operating in a good DCM mode.

From Fig. 3.6 and Fig. 3.7:

The load regulation is \( \frac{(1.2214-1.2036)}{(1-0.1)} = 19.8\text{mV/mA} \)

The line regulation is \( \frac{(1.2214-1.2128)}{(0.9-0.204)} = 12.4\text{mV/V} \)

The Maximum efficiency is 83%
The TVS boost converter operates in PFM, and when the input supply voltage is very low (200mV) and the load current is very high (1mA), the converter switches faster, and the maximum switching frequency occurs at the boundary of CCM and DCM. The highest and lowest switching frequency is 700kHz and 15kHz respectively. In addition, the maximum output ripple voltage is 24mV which is 2% of $V_o$. 

![Switching frequency vs. $V_s$](image1)

![Output ripple vs. $V_s$](image2)
The TVS boost converter has been successfully implemented and examined, and the performance of threshold voltage startup and low voltage input are the same as simulated results. However, the maximum efficiency is reduced by 3% comparing with simulation, which may due to the unexpected noise occur in the inductor current that increases the true r.m.s. (root-mean-square) of the input current. The overall performance of the converter is summarized in Table 3.1.

<table>
<thead>
<tr>
<th></th>
<th>Simulation</th>
<th>Measurement</th>
</tr>
</thead>
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<tr>
<td>Technology</td>
<td>AMS 0.35μm CMOS process</td>
<td>AMS 0.35μm CMOS process</td>
</tr>
<tr>
<td>Inductor</td>
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<td>4.7μH</td>
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<tr>
<td>Filtering capacitor</td>
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<td>500nF</td>
</tr>
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<td>Switching frequency</td>
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<td>7MHz (startup)</td>
</tr>
<tr>
<td></td>
<td>700kHz – 15kHz (PFM)</td>
<td>700kHz – 15kHz (PFM)</td>
</tr>
<tr>
<td>Input supply voltage</td>
<td>0.15V – 0.9V</td>
<td>0.15V – 0.9V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>1.2V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Output ripple voltage</td>
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<td>&lt;24mV</td>
</tr>
<tr>
<td>Load current</td>
<td>0.1mA – 1mA</td>
<td>0.1mA – 1mA</td>
</tr>
<tr>
<td>Efficiency</td>
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<td>Max. 83%</td>
</tr>
<tr>
<td>Line regulation</td>
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<td>12.4mV/V</td>
</tr>
<tr>
<td>Load regulation</td>
<td>12.4mV/mA</td>
<td>19.8mV/mA</td>
</tr>
</tbody>
</table>

Table 3.1: Summary of TVS BC’s performance
Chapter 4

Single-Inductor Dual-Input-Dual-Output (SI DIDO) Boost Converter

4.1 Overview of SI DIDO Boost Converter

In dealing with an intermittent energy source, we may add a rechargeable energy storage element to the system. When the energy harvesting source (for example, a piezoelectric device) is available, it supplies energy to the load, and at the same time, charges up the energy storage component (a rechargeable battery or a super-capacitor). When the source is not available, the energy storage component is reconnected as the input to maintain a continuous supply of energy to the load.

From the above discussion, a dual-input-dual-output (DIDO) converter is needed. In particular, we may employ time multiplexing and uses only one inductor to save off-chip components, and the single-inductor dual-input-dual-output (SI DIDO) boost converter is shown in Fig. 4.0. We assume that the source is available most of the time with only regular short breaks. One application is an energy harvesting scheme installing in the shoes, and the action of the SI DIDO boost converter is shown in Fig. 4.1. Several novel features are implemented. (1) The input power
MUX is driven by an internal charge pump for a larger gate drive to save area. (2) A 1:7 timeslot scheduling with a fixed peak inductor current is adopted for the two outputs with a large difference in load currents. (3) A time-multiplexing control loop is proposed to save on-chip components. (4) A new ramp generator is proposed that is suitable for sub-mW application. (5) The power stage is implemented with ringing suppression for the inductor and active diode core for controlling the PMOS power transistors. (6) The introduction of power-in-power-out concept and its application.

Fig. 4.1: Operation flow of SI DIDO boost converter
Traditionally, voltage conversion with two outputs is achieved by two DC-DC converters, as shown in the top diagram of Fig. 4.2. For low power applications, time multiplexing for the loads could be employed to eliminate L1 and S1, and a single-inductor dual-output converter could be used [Ma 01]. By time multiplexing the inputs, a single-inductor dual-input dual-output converter is proposed [Lam 03].
4.2 Analysis of SI DIDO Boost Converter

4.2.1 Comparison between SISO and SIDO

Fig. 4.3 shows the general operation flow of the single-input single-output (SISO) converter. In general, the output voltage \( V_o \) of converter is scaled down to \( bV_o \) to be compared with the reference voltage \( V_{ref} \) by the error amplifier (Error Amp), and the output of the Error Amp is compared with the ramp signal to generate the correct duty cycle for the power transistor in the power stage.

Fig. 4.4 shows the general operation flow of the single-input dual-output (SIDO) converter. Some functional blocks are shared by the two sub-converters such as \( V_{ref} \), clock and ramp signal. The power stage has to be modified and an additional time multiplexing input selector and controller are needed.

4.2.2 Internal potential allocation

Appropriate internal potential allocation can prevent latchup, uncontrollable startup and improve the efficiency of the converter. There are two voltage selectors in the power stage for choosing the highest voltage among \( V_{in1} \), \( V_{oa} \) or \( V_{ob} \) to bias the bulk terminals of all PMOS power transistors to prevent latchup, and to use as the gate drive of all PMOS power transistors to achieve a high efficiency.

One voltage selector picks the highest voltage of \( V_{in1} \) and \( V_{in2} \), prior to the MUX, to power up the internal control logic of the power stage to make sure that the logic is started before the startup of the converter. A second voltage selector after the MUX is
used to choose the highest voltage of $V_{in1}$ and $V_{in2}$ too to power up the charge pump of the MUX, such that the response of MUX is fast during the handover between $V_{in1}$ and $V_{in2}$. Two voltage selectors are used to prevent large switching noise from the charge pump to affect the logic controller in the power stage.

### 4.2.3 Elaboration of operation of DIDOBC

![Circuit Diagram](image)

The SI DIDO boost converter consists of two sub-converters. The NMOS power transistor $M_N$ is shared by both sub-converters, while the PMOS power transistors $M_{Pa}$ and $M_{Pb}$ are used to control $V_{oa}$ and $V_{ob}$ respectively. Since $V_{ob}$ supplies a much larger power than $V_{oa}$, $M_{Pb}$ switches 7 times as much as $M_{Pa}$ for a 8-clock cycle. If the peak inductor currents are kept the same for the two sub-converters, $V_{ob}$ can supply 7 times as much power as $V_{oa}$. Logic 1 and Logic 2 are used to decode the clk/8 signal for controlling $M_{Pa}$ and $M_{Pb}$.
The SI DIDO boost converter is designed to operate in DCM. Both outputs $V_{oa}$ and $V_{ob}$ are scaled down to $bV_{oa}$ and $bV_{ob}$ respectively, and the scaled outputs are compared to $V_{ref}$ by error amplifiers with compensation networks. Signals $V_{aa}$ and $V_{ab}$ are compared to the ramp signal and create two duty cycles, and two set-dominant RS-FFs are connected to the output of the comparators $Cua$ and $Cub$ respectively. The duty cycles are sent to the N-control block to control $MN$. Finally, the $cur\_over$ block monitors the inductor current $I_L$ and turns $MN$ off when it reaches the maximum set value.

Both sub-converters operate in DCM, and $MN$, $MPa$ and $MPb$ are all turned off when $I_L$ drops to zero. When such case occurs, ringing suppression switches $Min$ and $Mip$ are turned on to short out the inductor.

$V_{sin}$ is the selected power supply for the logic (within the dotted line) in the power stage, and $V_{bp}$ is the highest potential in the power stage that is used to bias $MPa$ and $MPb$. The signals $V_{12e}$ and $V_{24e}$ are the enable signals of $V_{oa}$ and $V_{ob}$ respectively. When the source is temporary not available, $V_{12e}$ is used to turn $MPa$ off. At the same time, the power MUX chooses $V_{in2}$ ($V_{oa}$) as the power input. When the system that follows the converter is turned off, $V_{24e}$ is used to isolate the system which is consuming power from $V_{ob}$. Therefore, the control to $V_{oa}$, $V_{ob}$ and to choose $V_{in1}$ or $V_{in2}$ as the input source are totally independent of each other. This flexibility is quite suitable for portable devices.

### 4.2.4 Power inout concept

Since $V_{oa}$ is the only node that could be connected to either the input or the output of the converter, this node is defined as the power inout node of the converter.
4.2.5 Error amplifier, loop gain and compensation

Fig. 4.6: Circuit diagram of error amplifier

Fig. 4.7: Simulation of frequency response of amplifier

Fig. 4.6 shows the amplifier that is used to compare \( bV_o \) with \( V_{\text{ref}} \). A two-stage amplifier with miller compensation is used. The sizes of \( M_1 \) and \( M_2 \) are larger than other transistors in the amplifier to reduce the input offset voltage. The simulation result of the amplifier is shown in Fig. 4.7. The dc gain is about 95dB, the unity-gain bandwidth is 6.8MHz with a phase margin of 78°. The switching frequency of the converter is 300kHz, much lower than the unity-gain bandwidth of the amplifier, and the amplifier can be considered as a single-pole system in designing the compensation network.
As both sub-converters work in DCM, there is no cross-regulation between the two outputs. One of the possible time-scheduling schemes of the inductor current is shown in Fig. 4.8. Volt-second balance equation of the boost converter gives

\[ V_1D_1 = (V_o - V_s)D_2 \]

and \( M = \frac{D_1}{D_2} + 1 \), where \( M = \frac{V_o}{V_s} \), the conversion ratio of the converter.

According to Fig. 4.9, for the sub-converter with output \( V_{oa} \), the charge \( Q_a \) delivered by the inductor within the clock period belongs to \( V_{oa} \) is

\[ Q_a = \frac{1}{2} \cdot \frac{V_s}{L} \cdot D_{1a} \cdot T \cdot D_{2a} \cdot T \]
Similarly, for the sub-converter with output $V_{ob}$, the charge $Q_b$ delivered by the inductor at the clock period that belongs to $V_{ob}$ is

$$Q_b = \frac{1}{2} \frac{V}{L} D_{1b} T \cdot D_{2b} T$$

As $V_{oa}$ only occupies 1 clock period per 8 clock periods, the output current $I_a$ is

$$I_a = \frac{1}{8T} \frac{Q_a}{V} = \frac{1}{16} \frac{V}{L} D_{1a} T \cdot D_{2a} T \cdot \frac{1}{8T}$$

$$\Rightarrow I_a = \frac{1}{16} \frac{V}{L f_s} D_{1a} D_{2a}$$

$$\Rightarrow I_a = \frac{1}{16} \frac{V}{L f_s} D_{1a}^2 \left( \frac{1}{M_a - 1} \right)$$

where $f_s$ is the switching frequency of clock, and $M_a$ is the conversion ratio of $V_{oa}$.

Similarly, $V_{ob}$ occupies 7 clock periods per 8 clock periods, and the output current $I_b$ of $V_{ob}$ is

$$I_b = \frac{7}{8T} \frac{Q_b}{V} = \frac{7}{16} \frac{V}{L f_s} D_{1b}^2 T \cdot \frac{7}{8T}$$

$$\Rightarrow I_b = \frac{7}{16} \frac{V}{L f_s} D_{1b}^2$$

Thus, the average power of $V_{oa}$ and $V_{ob}$ are

$$P_a = V_{oa} \cdot I_a = \frac{1}{16} \frac{V}{L f_s} \frac{D_{1a}^2}{M_a - 1} M_a$$

$$P_b = V_{ob} \cdot I_b = \frac{7}{16} \frac{V}{L f_s} \frac{D_{1b}^2}{M_b - 1} M_b$$

The maximum power from the converter is

$$P_{total} = P_a + P_b = \frac{1}{16} \frac{V}{L f_s} \left( \frac{D_{1a(max)}^2}{M_a - 1} + \frac{7D_{1b(max)}^2}{M_b - 1} \right)$$

with

$$M = \frac{D_{1(max)}}{D_{2(max)}} + 1 = \frac{1}{1 - D_{1(max)}}$$

Thus,

$$P_{total} = P_a + P_b = \frac{1}{16} \frac{V}{L f_s} \left( \frac{M_a - 1}{M_a} \right)^2 M_a + \left( \frac{M_b - 1}{M_b} \right)^2 7M_b$$
Chapter 4 Dual-Input-Dual-Output Boost Converter for portable application

\[ T(s) = A(s) \cdot h(s) \]

\[ T = \frac{1}{16} \cdot \frac{V_s^2}{L f_s} \left( M_a + 7 M_b - 8 \right) \]

Since output \( V_{oa} \) and \( V_{ob} \) are isolated from each other, they can be treated as outputs of two independent converters. The loop gain of each output is simply the loop gain of a single-input single-output boost converter in DCM, and is given by [Tam 99]

\[ T(s) = A(s) \cdot h(s) \]

\[ = A(s) b \frac{2V_o}{V_m (2M-1)} \sqrt{\frac{M-1}{KM}} \cdot \frac{1+ s \frac{R_{ESR} C_o}{2M-1}}{1+s \frac{M-1}{2M-1} \cdot R_o C_o} \quad (4.1) \]

where \( A(s) \) is the transfer function of amplifier with the compensation network, \( h(s) \) is the control-to-output transfer function of the converter, \( b \) is the scaling factor, \( R_o \) is the output loading resistor, \( C_o \) is the output filtering capacitor, \( R_{ESR} \) is the ESR, \( V_m \) is the peak-to-peak voltage of ramp signal, \( K = \frac{2L}{R_o T_e} \) where \( T_e \) is the equivalent clock period of each output. Thus, assuming \( T \) is the period of clock signal, \( T_e \) of \( V_{oa} \) is 8T. In addition, according to Fig. 4.10, \( T_e \) of \( V_{ob} = 8T/7 \), because the pattern of the inductor current related to \( V_{ob} \) is periodic, and after averaging the inductor current pattern, \( T_e \) is little bit larger than \( T \), which is 8T/7.

From equation (4.1), there are a low frequency pole and a high frequency zero at the control-to-output function \( h(s) \) in each output. The low frequency pole is at \(-\frac{2M-1}{(M-1)R_o C_o}\) and the high frequency zero is at \(-\frac{1}{R_{ESR} C_o}\). To make sure that the converter is stable, an amplifier with pole-zero compensation \( A(s) \) that has a low
frequency zero and high frequency pole is needed.

\[
A(s) = \frac{1 + s c_2 r_2}{s(c_1 + c_2) r_1 \left[ 1 + s (c_1 || c_2) r_2 \right]}
\]

where the low frequency zero is at \(-\frac{1}{c_2 r_2}\), the high frequency pole is at \(-\frac{1}{(c_1 || c_2) r_2}\)

and the first pole is at 0. The low frequency pole \(-\frac{2M - 1}{(M - 1) R_o C_o}\) of h(s) changes with the load current, and the low frequency zero \(-\frac{1}{c_2 r_2}\) generated by A(s) is fixed.

If the maximum load current is less than 10 times of the minimum load current, the converter is stable for all condition. Fig. 4.12 shows how the low frequency zero and the high frequency pole of A(s) compensating the low frequency pole and the high frequency zero of h(s) respectively. The phase margin of converter is 80° and 88° for V_{oa} and V_{ob}. 
From Fig. 4.12 and Fig. 4.13, the overall loop gain responses of the sub-converters are similar to a single pole system. Fig. 4.13 shows that the unity gain bandwidth of sub-converter V_{oa} is faster than that of V_{ob}.

### 4.2.6 Circuit implementation of SI DIDO boost converter

#### 4.2.6.1 Voltage selector

![Circuit diagram of Voltage selector](Lam03)
One voltage selector is the same as [Lam 03], where the highest voltage of $V_{in1}$ and $V_{in2}$ is selected and passed to $V_{out}$. When $V_{in1}$ is higher than $V_{in2}$, the gate of the PMOS transistor connected to $V_{in1}$ gets a low voltage and the gate of the PMOS transistor connected to $V_{in2}$ gets a high voltage, and $V_{out}$ is then connected to $V_{in1}$. A similar mechanism connects $V_{out}$ to $V_{in2}$ when $V_{in2}$ is higher than $V_{in1}$. This voltage selector cannot choose between $V_{in1}$ and $V_{in2}$ freely.

4.2.6.2 Level shifter

![Circuit diagram of level shifter](MA 03)

The level shifter shown in Fig. 4.15 is used to transfer the logic state from a low voltage circuit to a high voltage one, and the simulation result is shown in Fig. 4.16. This circuit is applied to both $M_{pa}$ and $M_{pb}$ and the power MUX. Note that the controller of $M_{pa}$ and $M_{pb}$, and the power MUX is supplied by 1V or 1.2V, while the outputs are 2.4V and 3.6V respectively. Therefore, level shifter is needed.
### 4.2.6.3 Peaking current source

![Circuit diagram of peaking current source](image)

Peaking current source is used for biasing and is shown in Fig. 4.17. This current source is suitable for low power and low voltage design because the minimum supply voltage is just $V_{gs4} + I_aR_b + |V_{ds1}|$. Assume the current level in this current source is very low and $V_{gs4}$ is close to $V_{th}$ (0.6V), $I_aR_b$ is close to zero and $|V_{ds1}|$ is close to 0.2V, the minimum supply voltage is 1V. Moreover, $I_a$ is independent of supply voltage. As this current source has two stable states, a startup circuit is needed. Several current sources are connected to different function blocks to reduce crosstalk among them.

Separated current source can reduce crosstalk among different function blocks, but the current matching is worse and also extra silicon area is needed. In fact, many of the function blocks do not need good current matching and extra active area is very small compared to the rest of the circuit.
### 4.2.6.4 Ramp and clock generator

![Fig.4.18: Circuit diagram of low potential comparator](image1)

![Fig.4.19: Circuit diagram of high potential comparator](image2)

![Fig.4.20: Circuit diagram of current mirror amplifier with pmos input stage](image3)

![Fig.4.21: Circuit diagram of current mirror amplifier with nmos input stage](image4)

![Fig.4.22: Circuit diagram of the ramp and clock generator](image5)

The ramp and clock generator is shown in Fig. 4.22. It assumes a conventional design, but uses common gate amplifiers as comparators for high speed, low voltage and low power.

From Fig. 4.18 to Fig. 4.21, the amplifiers with labels “p” and “n” are current mirror amplifiers with PMOS and NMOS input stage respectively. The amplifiers
with labels “l” and “h” are "low voltage sensing" and “high voltage sensing” input stages respectively. This ramp and clock generator can generate a wide range ramp signal (0.15V to 0.9V) with a low voltage supply of 1V.

Fig. 4.18 shows the low voltage sensing comparator with an input common mode voltage as low as one \( V_{ds(sat)} \) above ground. It is essentially a current comparator, when the input voltage \( V_{i+} \) is higher than \( V_{i-} \), the drain current of \( M_{i1} \) is smaller than that of \( M_{i2} \). The drain current of \( M_{i1} \) is mirrored to the output node \( V_o \), where \( M_3 \) could not source enough current for \( M_{i2} \) to sink, and hence \( V_o \) rises to put \( M_3 \) in the triode region. A similar argument applies for the case when \( V_{i-} \) is lower than \( V_{i+} \).

Fig. 4.19 shows the high voltage sensing comparator with an input common mode voltage as high as one \( V_{ds(sat)} \) below \( V_{dd} \). The working principle is the same as the low voltage sensing comparator. Note that for both comparators the input transistors are biased with top and bottom current sources of the same magnitude, and hence \( V_{i+} \) and \( V_{i-} \) do not need to draw a large current to induce a change. To further ensure that these comparators do not draw any current from node \( vh \) and node \( vl \) of Fig. 4.22, two current mirror amplifiers with PMOS or NMOS input stages connected as unity gain buffer are used (Fig. 4.20 and Fig. 4.21).

The ramp capacitor and the charging current have to be large enough to ensure an accurate clock frequency so as not to be affected by parasitics. The charging current is small and the discharging current is large, and the ramp signal assumes a sawtooth waveform. When the ramp signal is compared with \( vh \), the slow path of comparator is used, and when it is compared with \( vl \), the fast path of comparator is used. The frequency of ramp and clk signal is approximately equal to 
\[
\frac{V_{ref} r}{(vh - vl)R_{ramp} \cdot C_{ramp}}
\]
Fig. 4.23: Simulation of ramp generator

Fig. 4.23 shows the simulation result of ramp generator. The whole ramp generator only consumes an average of 3μA with a supply voltage of 1V to 1.2V, and the frequency changes from 272kHz to 280kHz, a mere 3% change. The output voltage of the ramp is nearly a rail-to-rail signal that reduces sensitivity to comparators’ input offset.
4.2.6.5 Clock divider

The SI DIDO converter is designed to operate in DCM, and the most efficient implementation is to design the converter to operate near the boundary of DCM and CCM when the output current is the largest, such that the peak inductor current could be reduced to reduce conduction loss. For the converter, one output is for the load and the other is for the rechargeable battery. The load works with 2.4V with high current and the rechargeable battery needs 1.2V with low current. To deal with two loads that have a large difference using a fix peak inductor current, the unbalanced time multiplexing scheme [Ma 03] could be used. Fig. 4.25 shows the clk-div-8.
block that allocates different time schedules for different outputs using leading-edge triggered clock dividers (clk-div) shown in Fig. 4.24. Fig. 4.26 and Fig. 4.27 shows that the clk-div-8 block allocates one cycle of an 8-cycle period for the light load and seven cycles for the heavy load.

4.2.6.6 Comparator

As the ramp of the converter is a nearly rail-to-rail signal, a comparator with rail-to-rail input common mode range is needed. Fig. 4.28 show a comparator that consists of two sub-comparators. For the L.H.S. sub-comparator, the input common mode range (ICMR) is from \( V_{dd} - |V_{ds(sat)}| - |V_{tp}| \) to gnd. For the RHS sub-comparator, the ICMR is from \( V_{dd} \) to \( V_{tn} + V_{ds(sat)} \).

Fig. 4.29 shows the proposed comparator by removing the current source part of its sub-comparators. For the L.H.S. sub-comparator, the ICMR is from \( V_{dd} - |V_{tp}| \) to gnd. For the R.H.S. sub-comparator, the ICMR is from \( V_{dd} \) to \( V_{tn} \). Hence, the input common mode range is enhanced by two \( V_{ds(sat)} \). For a 1V supply and assume that \( |V_{ds(sat)}| = 0.2V \), the two \( V_{ds(sat)} \) enhancement is almost a 40% improvement. The penalty is that the current consumption of the proposed comparator changes with the input common mode voltage. The maximum current consumption occurs when the input common mode voltage is either \( V_{dd} \) or gnd, and the speed determines the minimum current needed.

Note that if the threshold voltages are 0.7V, then the ICMR of the LHS
sub-comparator is 0.3V to 0V, and the ICMR of the R.H.S. sub-comparator is 1V to 0.7V. A dead band exists between 0.7V and 0.3V. In such a case, both the input transistors of the sub-comparators work in the sub-threshold region. If the minimum current is designed for the sub-threshold region, then the comparator could be considered as a rail-to-rail comparator.

Fig.4.30: Simulation of response of comparator

From the simulation result shown in Fig. 4.30, the comparator has better performance when either the PMOS or the NMOS input stage is working in the saturation region.
4.2.6.7 MUX (power mux)

The proposed MUX consists of a small on-chip 5x charge pump, control logic and power transistors. The power MUX uses only PMOS power transistors, the gate drive voltage is too low and a very large transistor is needed for low conduction loss. The 5x charge pump is used to generate a high voltage $V_{cp}$ for driving NMOS power transistors. Because the gate drive voltage is high and the mobility of NMOS transistors is larger than PMOS transistors, the area needed is much smaller. The calculation is as follows.
Chapter 4 Dual-Input-Dual-Output Boost Converter for portable application

For a PMOS power transistor:

\[ I_1 = \mu_p C_{ox}(W/L)_p[(|V_{gs1}| - |V_{tp}|)|V_{ds1}| - \frac{1}{2}|V_{ds1}|^2] \]

\[ \approx \mu_p C_{ox}(W/L)_p[|V_{gs1}||V_{ds1}|] \]

For a PMOS power transistor:

\[ I_2 = \mu_n C_{ox}(W/L)_n[(V_{gs2} - V_{tn})V_{ds2} - \frac{1}{2}V_{ds2}^2] \]

\[ \approx \mu_n C_{ox}(W/L)_n(V_{gs2} - V_{tn})V_{ds2} \]

Let \( V_{in1} = 1V, V_{in2} = 1.2V, V_{tn} = |V_{tp}| = 0.7V, V_{cp} = 3.6V \) and \( \mu_n = 3\mu_p \)

For \( I_1 = I_2 \) and \( |V_{ds1}| = V_{ds2} \):

\[ \Rightarrow \mu_p C_{ox}(W/L)_p(1.2 - 0.7) = \mu_n C_{ox}(W/L)_n(3.6 - 0.7) \]

\[ \Rightarrow (W/L)_p/(W/L)_n = 3(2.9)/0.5 \]

\[ \Rightarrow (W/L)_p/(W/L)_n = 17.7 \]

Thus, the size of a PMOS power transistor is about 17.7 times of the size of an NMOS power transistor using a charge pump is used. Therefore, using a charge pump is justifiable if the overall area needed is much reduced.

Fig. 4.31 shows the voltage selector that chooses the highest voltage of \( vin1 \) and \( vin2 \) as the supply voltage for the charge pump and the logic for the power MUX. The 5x charge pump in Fig. 4.33 provides the gate drives to the power transistors. The output \( V_{cp} \) is limited to 3.6V to avoid device breakdown. The charge pump is turned on or shut down depending on whether \( V_{cp} \) is higher than 3.6V or not. When \( V_{cp} \) is higher than 3.6V, the scaled \( V_{cp} \) is then higher than \( V_{refcp} \), and the comparator gives a cut-off signal to the 5x charge pump, otherwise, a turn on signal is issued.

Fig. 4.32 shows the clock generator for the 5x charge pump. When node enable is “0”, the clock generator issues clock signals to the pumping chain of Fig. 4.33 and pumps \( V_{cp} \) up. When node enable is “1”, node a is forced to “0”, \( \Phi_2 \) and \( \Phi_1 \) are forced to “1” and “0” respectively, making node v4 of the pumping chain high, and prevents reverse current of \( V_{out} \) from flowing back. Note that level shifters have to be
used for the low voltage control signal $V_{sel}$.

Fig. 4.34 shows the simulation results that verifies the calculation at the beginning of this sub-section. In our SI DIDO converter, the size of the NMOS power transistor in the MUX is $50000\mu/0.35\mu$, when the input voltage of the MUX is 1V, the output voltage of the MUX is 0.965V when the current is 0.85A. Thus, the maximum efficiency can never exceed 96.5%. The improvement of the output voltage of the MUX is less than 1% even the size of NMOS power transistor is doubled.

Fig.4.34: Simulation of performance comparison of switch that consists of NMOS with change pump and PMOS only

The 5x charge pump, voltage selector, control logic and feedback resistors of the charge pump only consume half of the chip area of the NMOS power transistor in the MUX. As there are two NMOS power transistor in this MUX, the total area is 2.5 times of an NMOS power transistor. Compared to $17.7 \times 2 = 35.4$ units if PMOS power transistors are used, the saving is 14 times.
4.2.6.8 Over current sensor (cur_over)

Fig. 4.35: Circuit diagram of current sensor

Fig. 4.36: Simplified circuit diagram of current sensor

Fig. 4.35 shows the current sensor modified from [Ma 03]. The current sources \( M_{b1} \) and \( M_{b2} \) provide the same current to bias \( M_{a1} \) and \( M_{a2} \). When node \( V_x \) increases, \( V_{gs} \) of \( M_{a1} \) decreases and node 1 is pulled up by \( M_{b1} \). When node \( V_{sense} \) increases, \( V_{gs} \) of \( M_{a2} \) does not change with the constant current biased by \( M_{b2} \), increasing of node \( V_{sense} \) pulls node 3 up and increases \( V_{gs} \) of \( M_{a1} \), node 1 is then pulled down by \( M_{a1} \). Thus, \( M_{a1}, M_{a2}, M_{b1} \) and \( M_{b2} \) form a differential amplifier with \( V_x \) as a positive input, \( V_{sense} \) as a negative input and node 1 is the output of this amplifier.

The current sensor could be simplified as shown in Fig. 4.36. When \( V_x \) increases, node 1 increases, \( V_{gs} \) of \( M_{sen} \) increases and the current flow to \( M_{cop} \) increases. At the same time, node \( V_{sense} \) and node 1 decreases.
Assume the bias current of \( M_{b1} \) and \( M_{b2} \) in Fig. 4.35 is much smaller than the inductor current, when \( M_N \) is turned on, its \( V_{ds} \) and \( V_{gs} \) are same as those of \( M_{cop} \). Now, \( M_N : M_{cop} = N : 1 \), implies \( I_d(M_N) : I_d(M_{cop}) = N : 1 \), and \( I_d(M_{cop}) \) is copied to \( R \) by the current mirror \( M_{s1} \) and \( M_{s2} \). Thus, the current sensor gives a signal “1” when \( I_L R/N = V_{refc} \). The supply of the current sensor is the input to the SI DIDO converter, which is 1V to 1.2V.

One limitation of the current sensor is the current mirror \( M_{s1} \) and \( M_{s2} \). If \( M_{s1} \) and \( M_{s2} \) are small, the response of current copying is fast. However, small \( M_{s2} \) requires a large \( V_{gs}(M_{s2}) \) to copy \( I_L/N \) to \( R \), and it limits the dynamic range of the voltage drop of \( R = V_{dd} - |V_{ds}(M_{s2})| \), where \( |V_{ds}(M_{s2})| > |V_{gs}(M_{s2})| - |V_{in}| \) to keep \( M_{s2} \) in the saturation region. Increasing \( W \) of \( M_{s1} \) and \( M_{s2} \) solves the above problem, but large \( M_{s1} \) and \( M_{s2} \) introduce large parasitic capacitance, and the response of current copying is slower.

### 4.2.6.9 N control block (with SD RS-FF)

![Fig. 4.37: Diagram of ports of N control black](image)

![Fig. 4.38: Conceptual circuit diagram of N control Block](image)

![Fig. 4.39: Circuit diagram of N control Block](image)
Fig. 4.40 shows the circuit and simulation result of the set-dominate RS Flip-flop, which is used to define the on-time of $M_N$ in each clock period. Fig. 4.37 shows the whole N control logic that processes all control signals for $M_N$. The core of the logic, the N control block, is shown in Fig. 4.38. At the beginning of each clock cycle, signal clk triggers the FF to give a signal to turn on $M_N$. Three on-times of $M_N$ are sent to the N control block, they are the upper bound of on-time defined by clk with current sensor, and both on-times that correspond to clk with both outputs. These on-times are known as $v_{sen}$, $sr24$ and $sr12$. Since clk/8 is used to schedule each time slot for both outputs, clk/8 is for heavy load that corresponds to $sr24$. The complement of clk/8 is for light load that corresponds to $sr12$. Enable signals $v_{24e}$ and $v_{12e}$ correspond to $sr24$ and $sr12$. Finally, the on-time of $M_N$ with correct time scheduling is combined with $v_{sen}$ to make sure that the maximum value of inductor current is well controlled. The exact implementation of the N control block is shown in Fig. 4.39.
4.2.6.10 Active diode core

Fig. 4.41 shows the active diode core that prevents the reverse current of the output PMOS power transistor. Take the sub-converter A as example. When the converter starts up, \( V_{oa} \) is low, and node c is mainly controlled by \( V_x \). Note that the bulk of PMOS power transistor \( M_{Pa} \) is connected to the highest voltage in the circuit \( V_{bp} \). When \( M_N \) turns on during start up, \( V_x \) is pulled down. Hence, \( V_d \) and \( V_s \) of \( M_{PA} \) are close to ground. Although \( V_{oa} \) is too low and node pg_in is low, \( M_{PA} \) does not turn on. When \( M_N \) turns on during start up, \( V_x \) is charged up the inductor current, pulling up node c and pg_in is "0", \( M_{PA} \) is then turned on and \( V_{oa} \) is charged up.

When the converter is in normal operation, \( M_b \) is biased by \( V_b \), and node c is mainly controlled by \( V_x \), as \( V_{oa} \) stays constant. When \( V_x \) is pulled down by turning on \( M_N \), it pulls node c down and node pg_in is pulled up and \( M_{PA} \) is turned off. When \( V_x \) is charged up by the inductor current, it pulls node c up, and node pg_in is pulled down and \( M_{Pa} \) is turned on.
4.2.6.11 P-control block (with logic 1 and 2)

Fig. 4.42: Circuit diagram of P control block

Fig. 4.43: Circuit diagram of Logic 1

Fig. 4.44: Circuit diagram of Logic 2

Fig. 4.45: Diagram of ports of P control block

Fig. 4.45 shows the whole P control block that controls both $M_{Pa}$ and $M_{Pb}$ for $V_{oa}$ and $V_{ob}$ respectively. Fig. 4.43 and Fig. 4.44 show logic 1 and logic 2 that work for $V_{oa}$ and $V_{ob}$ respectively. As mentioned before, clk/8 is for the 2.4V output $V_{ob}$, and the complement of clk/8 is for the 1.2V output $V_{oa}$. When v12e is pulled up and complement of clk/8 is pulled down, the 1.2V output is enabled and clkin of logic 1 is pulled up. When v24e and clk/8 are pulled up, the 2.4V output is enabled and clkin of logic 2 is pulled up.

Again, use $V_{oa}$ as example. Fig. 4.42 shows that clkin of logic 1 is used to select if pg_out should be connected to V_bp or pg_in inside the P control block. When $V_{oa}$ is enabled, clk in that corresponding to $V_{oa}$ is pulled up, pg_out of the P control block connects to pg_in, $M_{Pa}$ is controlled by the active diode core. However, when $V_{oa}$ is disabled in a particular time slot, clk in that corresponding to $V_{oa}$ is pulled down, pg_out of P control block connects to V_bp, the highest voltage of the converter, and $M_{Pa}$ is turned off.
4.2.6.12 Ringing suppression (M controller)

Fig. 4.46 shows the conceptual circuit diagram of the inductor mos control block. When $M_{Pa}$, $M_{Pb}$ and $M_N$ are turned off, the logic is to turn on $M_{in}$ and $M_{ip}$ in parallel with the inductor shown in Fig. 4.48 to suppress ringing.
4.2.6.13 Power buffer

The buffer of power MOS consists of a series of inverters as shown in Fig. 4.49. The starving transistor M₁ and M₂ operate in the linear region act as resistors to reduce the shoot through current of the inverter. The overall structure of the buffer is shown in Fig. 4.51. Simulation result of Fig.4.52 shows that the starving transistors greatly suppress the peak shoot through current by 10 times. This current suppression also reduces the glitches in the inductor current and at the output voltage.
Chapter 5

Simulation of SI DIDO

The single-inductor dual-input dual-output boost converter is implemented in AMS 0.35μm CMOS process and the layout is shown in Fig. 5.0. The chip measures 2245μm x 1345μm. In this chapter, the post-simulation results of the SI DIDO converter are shown to verify its functionality and performance.

Fig. 5.0: Layout view of SI DIDO
As mentioned previously, the control logic of the power stage is powered up first. Fig.5.1 shows that the power stage is well controlled at startup, and the maximum inductor current is limits at 850mA. $V_{cp}$ is controlled between 3.7V to 3.5V to give a good gate drive for the power transistors in the power MUX. The overshoots of $V_{oa}$ and $V_{ob}$ are 12% and 6% respectively, which is a little it large, but should be acceptable in most applications, because overshoots only occur for a very short time.
Chapter 5 Simulation of SI DIDO

Fig 5.2: Transient of output current of voa (cross regulation)

Fig 5.3: Transient of output current of vob (cross regulation)
Fig: 5.4: Transient of output current of both voa and vob

Fig: 5.5: Shut down of both voa and vob
Fig: 5.6: Shut down of vob

Fig: 5.7: Shut down of voa
Chapter 5 Simulation of SI DIDO

Fig: 5.8: Simulation of using v12e

Fig: 5.9: Simulation of using v24e
Fig. 5.10: Handover of supply (vs) of power stage verses vob

Fig. 5.2 and Fig. 5.3 show the load transient of $V_{oa}$ and $V_{ob}$ respectively. The power level of $V_{ob}$ is much higher than that of $V_{oa}$. Therefore, the transient of $V_{oa}$ did not affect $V_{ob}$, but the transient of $V_{ob}$ induced glitches to $V_{oa}$. In addition, Fig. 5.4 shows the transient simulation of both $V_{oa}$ and $V_{ob}$, proving that the converter is stable even when both outputs were changing at the same time.

Fig. 5.5 shows the simulation when both outputs are shut down. The inductor current was zero, and the converter was in good DCM behaviour. Moreover, Fig. 5.6 and Fig. 5.7 show that the converter delivered power to $V_{oa}$ and $V_{ob}$ respectively. When the converter delivered power to either one of the outputs, glitches appeared on the other output but the average change of the other output was less than 1mV. Therefore, the converter was able to deliver to any one output with little interference to the other output.

Fig.5.8 and Fig.5.9 demonstrate the functions of v12e and v24e. When either v12e or v24e was pulled high, the converter delivered power to the corresponding output $V_{oa}$ or $V_{ob}$. The inductor current was pulled to the maximum value when either v12e or v24e was pulled up, and the corresponding output was pulled up to the pre-set value similar to the startup of the converter, and the other output was affected,
because the inductor current was not guaranteed to go back to zero and cross-regulation occurred.

Fig. 5.10 shows the handover transient of source ($V_s$) of the power stage. When $V_{sel}$ is pulled down, MUX selected the rechargeable battery (1.2V) rather than the power from the energy harvester (1V).

Table 5.1 summarizes the simulation performance of the SI DIDO boost converter.

<table>
<thead>
<tr>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>AMS 0.35μm CMOS process</td>
</tr>
<tr>
<td>Inductor</td>
</tr>
<tr>
<td>2.2μH</td>
</tr>
<tr>
<td>Filtering capacitor</td>
</tr>
<tr>
<td>30μF</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
<tr>
<td>300kHz (Clock), 37.5kHz (voa), 262.5 (vob)</td>
</tr>
<tr>
<td>Input supply voltages</td>
</tr>
<tr>
<td>1V or 1.2V</td>
</tr>
<tr>
<td>Output voltages</td>
</tr>
<tr>
<td>1.2V or 2.4V</td>
</tr>
<tr>
<td>Output ripple voltage</td>
</tr>
<tr>
<td>&lt;42mV</td>
</tr>
<tr>
<td>Load current</td>
</tr>
<tr>
<td>5mA – 15mA (voa), 20mA – 80mA (vob)</td>
</tr>
<tr>
<td>Line regulation</td>
</tr>
<tr>
<td>10.6mV/V (vob)</td>
</tr>
<tr>
<td>Load regulation</td>
</tr>
<tr>
<td>0.2mV/mA (voa), 0.16mV/mA (vob)</td>
</tr>
<tr>
<td>Load transient response</td>
</tr>
<tr>
<td>(5mA to 15mA – voa) 0.5ms (voa)</td>
</tr>
<tr>
<td>(20mA to 80mA – vob) 1ms (vob)</td>
</tr>
</tbody>
</table>

Table 5.1: Performance summary of SI DIDO boost converter
Chapter 6

Conclusions and Future works

6.1 Example future work of TVS BC

Fig. 6.0: Circuit diagram of modified current sensor

Fig. 6.1: Plotting of $\Delta V$ v.s. inductor current

Fig. 6.2: Model of current adjusting part of Fig. 6.0

Fig. 6.1 shows that:

$$t_1 = \frac{L \cdot i_{t,max}}{V_s} \left( \frac{\partial i}{\partial t} = V \right)$$  \hspace{1cm} (6.1)

Where $i_{t,max}$ is Peak inductor current

$$D_1 M_1 = D_2 M_2$$

$$D_1 \frac{V_s}{L} = D_2 \frac{V_o - V_s}{L}$$

Thus,

$$t_1 \cdot V_s = t_2 \cdot (V_o - V_s)$$

$$t_1 \frac{V_s}{V_o - V_s} = t_2$$  \hspace{1cm} (6.2)

Charges that store in inductor are release to output capacitor at $t_2$, assuming
average output current is much less than the charging current from inductor to output capacitor at t2:

\[ C \cdot \Delta V = \frac{1}{2} \cdot \frac{V_o - V_s}{L} t_2 \cdot t_2 \]  

(6.3)

By sub both (6.1) & (6.2) into (6.3)

\[ \Delta V = \frac{1}{2C} \cdot \frac{V_o - V_s}{L} \left( \frac{V_s}{V_o - V_s} \right)^2 \left( \frac{L \cdot i_{L,\max}}{V_s} \right)^2 \]

\[ \Delta V = \frac{1}{2C} \cdot \frac{L}{V_o - V_s} \cdot i_{L,\max}^2 \]  

(6.4)

Thus, \( i_{L,\max} \propto \sqrt{V_o - V_s} \) with keeping constant \( \Delta V \)  

(6.5)

Fig.6.2 shows that:

\[ (w) \left[ \frac{V_s}{2} + |V_{gs}| \cdot V_{ih} \right] \cdot k_{i_{L,\max}} \cdot r_b - \frac{1}{2} \left( k_{i_{L,\max}} \cdot r_b \right)^2 \]

Where \( V_{ds} \) of mrp5 and mrp6 are small are they operate in linear region, because \( V_{rb} = k_{i_{L,\max}} \cdot r_b \) equals \( i_{L,\max} \cdot r_{on} \) where \( r_{on} \) is on resistance of N-power mos. Thus, current flow in \( r_b \) is related to inductor current flow on N-power mos.

\[ i - k_{i_{L,\max}} \approx \mu C_{ov} \left( \frac{w}{L_{nL}} \right) \left[ \frac{V_s}{2} + |V_{gs}| \cdot V_{ih} \right] \cdot k_{i_{L,\max}} \cdot r_b \]

\[ i - k_{i_{L,\max}} \approx k_1 \left[ \frac{V_s}{2} + k_1 \right] \cdot k_{i_{L,\max}} \cdot r_b \]

\[ i - k_{i_{L,\max}} = k_2 \left[ \frac{V_s}{2} + k_1 \right] \cdot i_{L,\max} \]

\[ i = i_{L,\max} \left[ k + k_2 \left( \frac{V_s}{2} + k_1 \right) \right] \]

\[ i_{L,\max} = \frac{i}{k + k_2 \left( \frac{V_s}{2} + k_1 \right)} \]

Where \( k_1, k_2 \) and \( k_n \) are some constants

\[ i_{L,\max} \propto \frac{1}{V_s} \]  

(6.6)

When (6.6) is compare with (6.5):
\begin{align*}
i_{L,\text{max}} & \propto \frac{1}{V_S} \left(\Delta V_o \right) \\
i_{L,\text{max}} & \propto \sqrt{V_o - V_S} \left(\Delta V_o \right)
\end{align*}

As \( k, k1 \) and \( k2 \) is chose and fitting well with \( C \) and \( L \) in (4), modified current sensor keeps \( \Delta V \) stay in almost constant with changing of \( V_S \) in certain range.

![Graph](image)

**Fig.6.3:** Plotting of \( V_o \) and inductor current of TVS BC with difference \( V_S \)

![Graph](image)

**Fig.6.4:** Simulation of \( V_o, V_S, \) inductor current and \( V_{node4} \) of original current sensor of TVS BC with 1mA loading

There is a minor problem exists in TVS BC, average \( V_o \) drops with dropping of \( V_S \). In boost converter, the magnitude of slope of rising ramp of inductor current is
and that of falling ramp of inductor current is \( \frac{V_o - V_s}{L} \). Decrease of Vs causes \( \frac{V_s}{L} \) decreases and the time for inductor to charge up to pre-set value increase. Moreover, \( \frac{V_o - V_s}{L} \) increases and the time for inductor current back to zero decreases. Therefore, the amplitude that Vo starts to ramp up in every cycle decrease, the duration of ramp up also decreases, and the final ramped up Vo amplitude decreases that is shown in Fig.6.3 and Fig.6.4.

The modified current sensor in Fig.6.0 solves the above problem. When Vs is decreases, potential on node r3 decreases, mrp3 sink more current, node r2 decreases, on resistance of mrp5 and mrp6 increases and current sink from mrp5 and mrp6 to node 4 decrease, potential on node 4 increases, pre-set peak inductor current increase to compensate the effect of decreasing of Vs. From Fig.6.5 and Fig.6.6, average value of Vo is improved and keeps almost steady from Vs equals 0.9V to 0.15V.

![Fig.6.5: Simulation of Vo, Vs, inductor current and V_{node4} of modified current sensor of TVS BC with 0.1mA loading](image-url)
Fig. 6.6: Simulation of $V_o$, $V_s$, inductor current and $V_{node4}$ of modified current sensor of TVS BC with 1mA loading.

Fig. 6.7: Simulation of Efficiency of TVS BC with original and modified current sensor.

In addition, Fig. 6.7 shows that inductor current increases with decreasing $V_s$ to compensate the effect of decreasing $V_s$. Increasing inductor current introduces an
additional conduction loss. Therefore, efficiency of TVS BC decreases with decreasing of $V_s$. There is a trade-off between efficiency and evenness of $V_o$.

### 6.2 Example future work of SI DIDO

Fig. 6.8: New cur\_over

Fig. 6.8 shows the new cur\_over which is modified from cur\_over in Fig. 4.35. Gate drive of N-power mos and current supply of cur\_over is coming from vs, however, gate drive of N-power mos and supply of new cur\_over is separated into vbp and vs.

The current bias part of cur\_over cannot be supplied by vbp, because range of vbp is varied too much (range of vbp is 1V to 2.4V), however, giving gate drive of N-power mos with vbp enhances the efficiency of converter by reducing the on-resistance of N-power mos. Therefore, cur\_over in Fig. 4.35 limits the efficiency of the converter with biasing the current supply and gate drive of N-power with vs only. And the efficiency of SI DIDO can be enhanced by using the new cur\_over.
6.3 Conclusions

As discussed before, exploding of portable devices for long lasting applications are not supported by existing batteries well. Moreover, used batteries also cause lots of environmental problems. On the contrast, energy harvesting technique provides a clean, recycling, and environmental friendly power source. Therefore, energy harvesting source is a good solution for portable applications with long lasting running time. However, special converters' designs for those energy harvesting sources are needed.

Two converters, TVS BC and SI DIDO for fluctuating source or not always available source are implemented with AMS 0.35um CMOS process respectively. The first converter is realized with measurement while the second is realized with post-simulation result. They are target to different application of energy harvesting source. The first one supports large input range with threshold voltage startup for sub-mA application, the second one supports dual-inputs and dual-outputs with MUX that includes build in charge pump in order to fully utilize the energy from energy harvesting source.

The first converter, Threshold voltage startup boost converter (TVS BC) can be started up with MOSFET threshold voltage of its fabrication process (0.65V) and converts a fluctuating power (i.e. solar cell) to regulated output (1.2V) with large input voltage range (0.2V to 0.9V) for sub-mA (loading current range is from 0.1mA to 1mA) applications. TVS BC operates in PFM with DCM mode, and the maximum efficiency is 83% with die area is 675μm x 615μm.

The second one, Dual-inputs-dual-outputs boost converter (SI DIDO) can fully utilize the energy from a source which is fairly constant but not always available (i.e. Piezoelectric source, 1V) to two regulated outputs for batteries charging (1.2V, 5mA to 15mA) and usage of system (2.4V, 20mA to 60mA) with fixed peak inductor
current (850mA) under 1 to 7 time multiplexing DCM mode. Therefore, the rechargeable batteries store the energy from the unstable source and provide energy to the system when the source is not available. In addition, the switching frequency of main clock is 300kHz, the converter also provides free matching of any one of inputs to any one of outputs with built-in MUX for different applications in portable devices, and its layout area is 2245μm x 1345μm.
References


