Figure 1.1: Transformation from surface mounted passives to embedded passives.
Figure 1.3: Stacked configuration of chip capacitor
Figure 3.2: Au/ BaTiO$_3$/Au/TH/W/Si sample for electrical testing.
Noise sealing

Figure 3.4 (a) Electrical testing configurations

Figure 3.4 (b) HP4284A LRC meter

Figure 3.4 (c) Probing station
Figure 4.1: Process flow for building hydrothermally treated BaTiO$_3$ film capacitor on PCB substrate.
Figure 4.7: SEM pictures of hydrothermal BaTiO$_3$ surface at 70°C with different treatment durations.
Figure 4.8: SEM pictures of hydrothermal BaTiO$_3$ surface at 90°C with different treatment durations
Figure 4.11: Cross section view of hydrothermal BaTiO$_3$ on Ti foil with 7 and 14 day treatment.