Fig. 2.2 Optical resist pattern after optical exposure process on different structures. (a) 1.2 μm NAND4 oscillator; (b) 1.2 μm XNOR oscillator and (c) L-Bar.
Fig. 2.3 The optical micrographs show the optical resist pattern after (a) 150 °C hardbake for 2 minutes and (b) 165 °C hardbake for 2 min. SEM micrographs show the optical resist profile (c) before hardbake and after (d) 165 °C hardbake.
Fig. 2.6 Optical resist pattern after F-plasma process, postbake and e-beam direct write process. (a) & (b) If the post-bake temperature is below 105 °C, the resist is eroded. (c) The post-bake temperature is 120°C and 1 min. (d) If the post bake temperature is 140 °C or above, the resist surface has crack on the large area pad.
Fig. 2.8 Mix and match pattern. (a) Optical resist before e-beam development; (b) optical and e-beam resist and matching after e-beam development; (c) magnified the optical and e-beam resist pattern to show the interface.
Fig. 2.9 Gate pattern after poly-Si etch, which is defined by optical lithography. (a) 1.2 μm NAND4 oscillator; (b) 1.2 μm XNOR oscillator and (c) L-Bar.

Fig. 2.10 Gate pattern after poly-Si etch, which is defined by e-beam direct write. (a) 0.2 μm NAND4 oscillator; (b) 0.2 μm XNOR oscillator.
Fig. 2.11 (a) & (c) Gate pattern after poly-Si etch, which is defined by 'Mix and match' after poly-Si etch and (b) magnified the interface between the optical and e-beam resist.
Fig. 3.3 The SEM photograph shows the cross-section of the 1:1 line / space resist profile after the Shipley is spun onto the PMMA. The interface between the Shipley and PMMA resist is not sharp due to the resist charging effect. The sample has been stointed with mild resist etching.

Fig. 3.4 The SEM photograph shows the regions of the Shipley and PMMA resists after the Shipley resist is spun onto the PMMA resist and etched back (the schematic diagram is shown in Fig. 3.1(c).)
Fig. 3.6 The SEM photograph shows the final Shipley resist pattern, using electron scanning and development to remove the PMMA.
Fig. 3.8 The SEM photograph shows the final Shipley resist pattern, using electron scanning technique. Some PMMA residue is left due to under exposure between two electron scanning beam lines.
Fig. 3.10 The SEM photographs show the final Shipley resist pattern, using DUV and development to remove the PMMA.
Fig. 3.11 The SEM photograph shows the cross-section of the final Shipley resist pattern.
Fig. 3.12 A gate electrode measuring with thin gate and large pad area.
Fig. 4.3  (a) The optical micrograph shows the recrystallization region after 560 °C annealing. The region that is outside the crystallization region receives annealing under Solid Phase Crystallization.  
(b) The size of recrystallized region is plotted with different annealing time and Ni seeding window width.  
(c) The recrystallized region width is plotted with different Ni thickness and window width.
Fig. 4.4 (a) Subthreshold characteristics of n-channel and p-channel MILC TFTs, with different 
$V_{th}$ and (b) $I_d - V_d$ characteristics. The effective channel length is 0.71 μm and channel 
width is 9.73 μm.
Fig. 4.5 Subthreshold characteristics of n-channel and p-channel MILC TFTs, with (a) channel width of 5.17 μm and various effective channel lengths $L$; and (b) effective channel length of 0.71 μm and various gate widths $W$. 
Fig. 4.6 Leakage currents of p-channel MILC TFTs, with different effective channel lengths $L_{\text{eff}}$ from 0.59 to 4.4 $\mu$m and different channel lengths $W$ from 0.3 to 5 $\mu$m. Long width and short channel devices have larger leakage current.
Fig. 4.7 Cumulative distributions of (a) subthreshold slope and (b) threshold voltage from p-channel MILC TFTs for various device effective channel lengths $L_{\text{eff}}$. 
Fig. 4.8 Cumulative distributions of (a) subthreshold slope and (b) threshold voltage from p-channel MILC TFTs for various device gate widths $W$. 
Fig. 4.11 Cumulative distributions of (a) subthreshold slope, (b) threshold voltage and (c) field effect mobility from p-channel MILC TFTs for different distances \(d_{ni}\) between the transistors and the nickel seeding window. All the devices have the same size, with effective channel length \(L_{eff}\) of 0.88 \(\mu\)m and gate width \(W\) of 4.41 \(\mu\)m. The small number in the graph indicates the transistor position \(d_{xo}\) (in \(\mu\)m) relative to the nickel-seeding window.
Fig. 4.12 (a) Subthreshold slope, (b) threshold slope and (c) field effect mobility from p-channel MILC TFTs with effective channel length $L_{\text{eff}}$ of 0.59 to 4.4 $\mu$m and gate width $W$ of 0.3 to 5 $\mu$m.
Fig. 4.14 Illustration of the device performance with different device gate lengths and widths. Larger the index, better the performance, closer to a single-crystallized device and smaller the variation. The device should be placed at least 10 μm from the Ni seeding window, and the Ni strip should be placed as in Type Ni_A.
Fig. 5.2 The SEM micrographs shows the silicon bridge structure after nitride etch (refer to Fig. 5.1(c)) or the schematic diagram.)
Fig. 5.3 The SEM micrographs of the GATs.
Fig. 5.4 NMOS and PMOS $I_d - V_g$ curves of MILC GAT and SGT, with SPC and convention SOI devices for comparison. $L_d/W_d$ = 0.55 / 0.47 μm.
Fig. 5.5 Transconductance ($\delta I_d / \delta V_g$) at $|V_{ds}| = 0.05$ V, with SPC devices for comparison. (a) NMOS and (b) PMOSFETs $g_m$, with $L_g / W_g = 0.55 / 0.47$ μm
Fig. 5.6 NMOS and PMOS $I_d - V_d$ curves of MILC GAT and SGT, with SPC and convention SOI devices for comparison. $L_g / W_g = 0.55 / 0.47 \ \mu m$. $|V_g - V_i| = 0, 1, 2, 3 \ \text{V}$. 
Fig. 6.2 The optical micrograph of a 3-D ring-oscillator. (a) The highlighted area shows the layout of the active, gate and the contact area for the NMOSFET (bottom layer) and PMOSFET (top layer). (b) Magnification of a 3-D inverter.
Fig. 6.3 (a) The layout showing the 2-D and 3-D inverters with fan-in equals one. (b) The relative layout area of each type of inverters. All the data are normalized to the overall area of the 2-D inverters.
Fig. 6.4 (a) The schematic diagram of the 3-D deep contact. (b) and (c) show the contacts under SEM, after 20 min dry oxide etch by CHF$_3$ and 10 min 10:1 dilute HF.
Fig. 6.6  Optical micrographs show different type of circuits. (a) XNOR ring-oscillator. (b) 4-bit shift register and (c) D Flip-Flop.
Fig. 6.7 (a) Optical micrograph shows the 3-D inverter structure, with the PMOS on the top and NMOSFET on the bottom layer. (b) SEM micrograph shows the 3-D inverter cross-section, where the top layer and bottom layer devices are not stacked. (c) - (d) Magnified the top and bottom layer devices.
Fig. 6.8 (a) An optical micrograph shows a 3-D inverter structure, with the PMOS on the top and NMOSFET on the bottom layer and are stacked. (b) SEM micrograph shows a 3-D inverter cross-section. (c) The structure is magnified.
Fig. 6.9  $I_d - V_g$ curves of the bottom and top layer devices, with $|V_{dd}| = 0.05$ V. bottom layer: $L / W = 0.54 / 4.3 \, \mu m$; top layer: $L / W = 0.71 / 5.2 \, \mu m$. 
Fig. 7.1 Transfer characteristics of (a) different types of inverters, with power supply of 3 V; (b) 3-D inverters, with different power supply from 0.5 to 3 V; (c) 3-D inverters of five different logic blocks, including INV, NAND2, NAND3, NAND4 and XNOR.
7.3 RING-OSCILLATOR AND CIRCUIT PERFORMANCE COMPARISON

Ring oscillators were fabricated. The optical micrograph is overviewed in Fig. 7.2 and the magnified picture can be referred to Fig. 6.2. They have 25 stages of inverters with fan-in and fan-out equal to 1, and large buffers at the output stage. The sizes of the transistors are same as those mentioned in the last section.

![Diagram of ring oscillator](image)

Fig. 7.2 (a) The schematic diagram and (b) optical micrograph of a 3-D INV oscillator (25 stages of inverters + output buffer).
Fig. 7.9 The optical micrographs of the 4-bit Shift Register. $X_1X_2X_3X_4X_5X_6X_1$ are inputs, $Y_1Y_3Y_2Y_1$ are outputs and $S_1S_2$ are address selectors.
Fig. 7.10  The CRO micrographs show the input data, address selector and output waveforms of a 3-D test circuit.
Fig. 7.17 Drive current of the (a) bottom and (b) top layer devices.

Fig. 7.18 The propagation delay of the 25-stage MILC / MILC 3-D ring-oscillator is compared to Fig 7.15.
Fig. 8.1 The SEM micrograph of the large grain poly-Si film, after (a) 560 °C and (b) 560 + 900 °C annealing.
Fig. 8.2 (a) The AFM image shows the surface roughness of the crystallization region near the Ni seeding window. (b) The average surface roughness is plotted along the diffusion path from the seeding window towards the MILC front.
Fig. 8.3  AFM picture shows the surface roughness of the single crystal tail-like region and the nearby rough surface.
Fig. 8.4 The grain boundaries and surface roughness of multiple crystallization regions are observed under (a) SEM and (b) AFM.
Fig. 8.5(a) shows the AFM images near the MILC front. The picture includes two regions, namely the MILC and SPC area. The MILC region has a smooth surface (Fig. 8.5(b)). The SPC region has a rough surface and lumps of grains can be observed (Fig. 8.5(c)).

Fig. 8.5  AFM picture shows the (a) MILC front, (b) MILC region and (c) SPC region.
Fig. 8.10 Cumulative distribution of experimental data from PMOS MILC TFTs with varying channel lengths. The result of SOI TFTs is also included for comparison.
Fig. B.3 The SEM micrographs after (a) poly etch and (b) spacer etch. The spacer width is ~750 Å.
Fig. B.5 The SEM micrographs after spacer etch and salicidation with different channel lengths.
Fig. B.6 SEM picture shows a Polycide gate with oxide spacer.
C.1 E-BEAM MIX-AND-MATCH LAYOUT
NMOSFET or PMOSFET
or buried channel PMOSFET
with different channel L and W,
Including narrow W
(Ni strip in Type Ni_B)

NMOSFET or PMOSFET

C.2 GATE-ALL-AROUND TRANSISTOR LAYOUT
C.3  3-D STRUCTURE LAYOUT

3-D inverters, inverter-chain, ring-oscillator

Type \( A \) inverters, inverter-chain, ring-oscillator

Type \( B \) inverters, inverter-chain, ring-oscillator

N莫斯FET lower layer

P莫斯FET lower layer

Type \( A \) inverter-chain inverters

Type \( B \) inverter-chain inverters

Shift register

N莫斯FET lower layer

P莫斯FET upper layer

3-D D-Flip Flop

Type \( A \) D-Flip Flop

Type \( B \) D-Flip Flop
Fig. D.3 The PMMA resist thickness with different coating spin speed (The thickness may change from time to time).

Fig. D.4  SEM micrographs show the PMMA (a) resist pattern viewed from the surface and (b) resist profile for different pattern dimensions.
Fig. D.6 Inappropriate clock and dose range are used. Some of the scattered electron beam exposes the gap between the two big patterns. The resist under this gap cannot be developed away. This is not due to under-development of resist. (a) Optical and (b) SEM micrographs.
Fig. D.7 The e-beam Shipley resist pattern. (a) 0.3 µm and (b) 0.2 µm designed gate length.

Fig. D.8 The SEM micrographs show different gate length pattern after polysilicon etch. The design gate lengths are (a) 0.15 µm, (b) 0.20 µm, (c) & (d) 0.30 µm.