The Impact of NQS Simulation on RF IC Design with a Particular Emphasis on Low Noise Amplifiers

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by

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November, 1998
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ABSTRACT

The continued improvement in speed in CMOS devices has prompted many to look into the possibility of building CMOS RF front-end circuits. While several research results have been presented recently on using CMOS technologies for building LNAs, there has been a substantial mismatch between simulation and measurement results. The push to design low cost RF IC in CMOS technologies has called for more scalable model that includes all advanced technology features and Non-Quasi-Static (NQS) effects.

The NQS effect of sub-micron MOS transistor was studied using MEDICI 2-D device simulation program. The accuracy of the latest BSIM3V3 NQS model was verified by using the model extracted from the MEDICI simulated DC current and capacitance data. A 2.4GHz LNA design was used to illustrate the impact of NQS effect on LNA architecture and performance. Device characterisation was performed on the 0.35μm MOS transistors. Based on the knowledge of NQS effect, a 2.4GHz LNA operating at a 1.5 volt power supply was fabricated using 0.35μm CMOS technology.
To

my dearest father and mother
Acknowledgments

Without the intellectual, physical and emotional support from many individuals, not only this thesis would not have been possibly completed, but also I could not have enjoyed my time at this university, where I have been growing to be an educated as well as a cultivated person during the last five years.

Firstly, I would like to especially thank my thesis supervisor, Dr. Jack Lau, not only for his technical support, but also for creating this particularly stress-free environment which provides a large degree of freedom for me to enjoy my studies and my research work. He also always shares his valuable experience and his intellectual maturity with me that all these are very useful for my future career. Next, I would like to thank Prof. Ping Keung Ko for all the advices. I would also like to thank Dr. Mansun Chan for advising on device simulation and modeling issues and Dr. Win-Hung Kit and Prof. Philip Chan for sitting on my thesis committee.

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CHAPTER 1  Introduction

1.1 Motivation

With the increasing popularity of wireless communication systems like Wireless-Local-Area-Network, wireless printer, and wireless audio system, higher levels of RF component integrations are required to reduce the size and cost of products. Low power consumption and compact design are the ultimate goal for portable wireless products such as wireless LAN for Laptop. Traditionally, RF components are dominated by gallium arsenide technology due to its excellent noise performance, high gain and high output power.
However, as shown in Fig. 1, CMOS technology is advancing at a fast pace. As the minimum feature size of CMOS scales toward the deep sub-micron region, great expectations are aroused for CMOS RF circuits at 1-2 GHz. Overcoming the dominance of silicon bipolar may become more plausible in this region. Using CMOS technology for RF components, full integration with base-band circuitry can be realized. However, there are still many issues that have to be understood, such as high frequency properties of CMOS device and interference.
between RF circuitry and base-band circuitry, before we can obtain the best performance. A scalable CMOS SPICE model that can handle the Non-Quasi-Static (NQS) effect is a key factor for optimal RF circuit design.

1.2 Background

When engineers use discrete transistors to implement RF circuits, it is very common and reliable to use measured s-parameters for circuit simulation. However, we do not have this luxury when we do monolithic microwave IC design using CMOS technology. SPICE is a widely used simulation tool, not only because it is easy to use but also SPICE models are generally provided by process vendors. The lack of accurate SPICE models at high frequency leads to sub-optimal circuit design.

1.2.1 LNA Architecture

Based on the knowledge of SPICE model and circuit theory, four different LNA architectures shown in Fig. 2 were used to fulfil the impedance matching requirement. In SPICE small signal model, gate and source are connected by a single capacitor. Since it is not possible to transform the pure reactive impedance to real impedance by a lossless matching network, resistive elements are used for impedance matching when the input of the LNA is the
gate as shown in Figs. 2(a) and 2(b). The major disadvantage of these matching techniques is the degradation in noise figure due to the additional thermal noise introduced by the matching resistors. The common-gate architecture shown in Fig. 2(c) can provide real input impedance

![Diagram of common LNA architectures](image)

**FIGURE 2.** Common LNA architectures. (a) Resistive Termination. (b) Shunt-Series Feedback. (c) $1/g_m$ Termination. (d) Inductive Degeneration.

for impedance matching but it suffers from unknown parasitics connected to the source input port [1]. The inductive source degeneration technique used in Fig. 2(d) is the most prevalent method used in GaAs MESFET amplifiers, and has also been used in CMOS amplifiers [2]. The source-inductive degeneration technique has been promoted that it can achieve the best
noise performance of any architectures [2] because it provide the real input impedance by ideally noiseless source inductor.

1.2.2 Limitation of commonly used SPICE models

Most commonly used SPICE MOS transistor capacitor model are based on Quasi-Static (QS) assumption except the latest version of BSIM3V3 model. The QS model assumes that the node charge will follow the node voltage variation instantaneously and ignore the finite charging time. The simulation accuracy is acceptable for digital circuit even at moderate frequency. The major reason is that the interconnecting wire dominate the delay time of the circuit. However, there still exists critical problems as discussed in [3]. In the analog circuit domain, this finite charging time introduce significant error in determine the phase margin of amplifier, phase noise of oscillator, and even the performance of narrowband amplifier such as LNA.

1.3 Research goal

In order to design an optimal LNA using the CMOS technology, the understanding of device characteristic is important. The non-quasi-static effect of the MOS transistor must be taken into consideration. We study the high frequency properties of the MOS transistor using
2-D device simulation program. Results reveal the limitation of current SPICE model accuracy on predicting NQS effect as comparing SPICE simulation results with 2-D device simulation results and to device measurement results. Based on the understanding of device properties and simulation models' limitation, we propose a simple LNA architecture which can achieve better performance.

1.4 Thesis outline

This thesis focuses mainly on the analysis of high frequency properties of sub-micron MOS transistor, current SPICE model limitations on predicting NQS effects, and the design procedure and testing results of a 2.4GHz LNA. Chapter 2 shows the comparison results of the high frequency characteristic of the bulk MOS device between MEDICI 2-D device simulation results and SPICE BSIM3V3 model simulation results. Chapter 3 presents the testing device layout and measurement results. Chapter 4 discusses the design and performance results of a 2.4GHz single-ended LNA. Finally, Chapter 5 presents some concluding remarks.
CHAPTER 2

High Frequency
Characteristic of Bulk
MOS Device

2.1 Introduction

Commonly used SPICE models are usually based on Quasi-Static assumption for transient and AC analysis. These models usually failed to predict the performance of analog circuit. For example, in order to predict the phase margin of an OpAmp, AC analysis has to be performed up to the cut-off frequency of the transistor. QS assumption is known to be invalid at this frequency. The NQS effect of long channel device has been studied analytically in [4] and [5]. These results are very complicated. They are either too difficult to be implemented in SPICE model or will increase the simulation time significantly [6]. As CMOS technology improves and runs into the sub-micron and deep sub-micron regime, the situation is even more complicated.
A simplified NQS model was introduced in the latest BSIM3V3 model [3]. However, in-depth analysis of model accuracy for RF circuit simulation are rarely reported. In here, the model was first verified by comparing the simulation results of an advanced device structure with 2-D device simulator MEDICI. MEDICI simulates the device behaviour by solving Poisson's equation and the electron and the hole current continuity equations in two-dimension [7]. The AC simulation is done by sinusoidal steady-state analysis under the DC bias condition. The frequency dependent admittance matrix, and then capacitance and conductance, are calculated from the sinusoidal terminal currents and voltages [7]. Unlike the charge partitioning methods used in other similar programs, this method is inherently non-quasi-static and the frequency limit depends on the grid size only.

2.2 2-D device simulation and BSIM3V3 model extraction

Since the exact approaches of different manufacturers to sub-micron scaling are often closely guarded secrets, the processing parameters from 0.15μm process [8] is used as a reference to create a MOS device structure for simulation. The primary goal is to have a realistic device for simulation such that the conclusions drawn from the simulation results are meaningful.
2.2.1 Doping profile of sub-micron LDD CMOS device from TSUPREM simulation

Several process parameters are required for device simulation. The most important one is the channel doping profile. The fabrication process conditions of the 0.15μm process [8] is listed in Table I.

<table>
<thead>
<tr>
<th></th>
<th>condition / value</th>
</tr>
</thead>
<tbody>
<tr>
<td>well</td>
<td>B⁺ 100 keV 4.0 x 10¹² cm⁻²</td>
</tr>
<tr>
<td>channel</td>
<td>B⁺ 70 keV 3.6 x 10¹³ cm⁻²</td>
</tr>
<tr>
<td></td>
<td>B⁺ 15 keV 5.0 x 10¹² cm⁻²</td>
</tr>
<tr>
<td>LDD N⁺</td>
<td>As 20 keV 2.0 x 10¹⁴ cm⁻²</td>
</tr>
<tr>
<td>source / drain</td>
<td>As 50 keV 5.0 x 10¹⁵ cm⁻²</td>
</tr>
<tr>
<td>tox</td>
<td>4.3 nm</td>
</tr>
<tr>
<td>sidewall</td>
<td>Si₃N₄ 100 nm</td>
</tr>
<tr>
<td>activation</td>
<td>RTA 1000 °C 20 sec</td>
</tr>
</tbody>
</table>

The final device structure from TSUPREM is shown in Fig. 3. For simplicity, an analytical channel doping profile close to the simulated doping profile was used for MEDICI simulation (Fig. 4). Other device parameters are summarized in Table II and the final device structure is shown in Fig. 5.
FIGURE 3. Cross-section view of the CMOS device from TSUPREM.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ox}$</td>
<td>7.6nm</td>
</tr>
<tr>
<td>gate length</td>
<td>0.4um</td>
</tr>
<tr>
<td>drain/source doping</td>
<td>1.3e21</td>
</tr>
<tr>
<td>drain/source junction depth</td>
<td>0.15um</td>
</tr>
<tr>
<td>lateral diffusion ratio (x/y)</td>
<td>0.6</td>
</tr>
<tr>
<td>LDD doping</td>
<td>1e20</td>
</tr>
<tr>
<td>LDD junction depth</td>
<td>0.05um</td>
</tr>
<tr>
<td>substrate doping</td>
<td>6.2e14</td>
</tr>
<tr>
<td>substrate thickness</td>
<td>5um</td>
</tr>
</tbody>
</table>
FIGURE 4. NMOS channel doping profiles simulated from TSUPREM and used in MEDICI simulation.

FIGURE 5. Cross-section of the 0.35um NMOS structure created in MEDICI.
2.2.2 D.C. node current and node capacitance from MEDICI simulation

To extract BSIM3V3 model, the test device are first characterized, at least, under different gate and drain voltages with different body biases. If the accuracy of the capacitance model is of concern, C-V data from drain, source and body to gate are also needed.

The I-V simulation in MEDICI is straightforward. Terminals voltage are limited below 3 volts as sub-micron devices are mostly used for 3-volt or less operation. Capacitance data are obtained by doing AC analysis at 10 Hz. Since the capacitance model in BSIM3V3 is charge conservation model and is described by

\[ C_{ij} = \frac{\partial Q_i}{\partial V_j} = \text{Im} \left( \frac{i}{\sqrt{V_j \cdot \omega}} \right) \bigg|_{\omega \to 0} \]  

(EO 1)

\[ C_{ij} \] is negative if \( i \) not equals \( j \).

2.2.3 BSIM3V3 model extraction

A commercial software called BSIMProTM is used to extract the BSIM3V3 model. The required input data are summarized in Table III. Some model extraction results are shown in Figs. 6 and 7. As expected, the DC I-V model of the BSIM3V3 are very accurate except the output resistance that error increases as Vgs decreases. Usually, a compromise have to be
TABLE III. Data required for BSIM3V3 model extraction.

<table>
<thead>
<tr>
<th>data</th>
<th>1st order</th>
<th>sweeping parameters</th>
<th>3rd order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Id-Vg</td>
<td>(V_{gs}=0) to (3\ V \ @0.1\ V)</td>
<td>(V_{bs}=0) to (-3\ V \ @-1\ V)</td>
<td>(V_{ds}=0.05\ V, 2\ V)</td>
</tr>
<tr>
<td>Id-Vd</td>
<td>(V_{ds}=0) to (3\ V \ @0.1\ V)</td>
<td>(V_{gs}=0.5) to (3\ V \ @0.5\ V)</td>
<td>(V_{bs}=0\ V, -1\ V)</td>
</tr>
<tr>
<td>Cgc</td>
<td>(V_{gs}=-3) to (3\ V \ @0.2\ V)</td>
<td>(V_{bs}=0) to (-3\ V \ @-1\ V)</td>
<td>(V_{ds}=0\ V)</td>
</tr>
<tr>
<td>Cgb</td>
<td>(V_{gb}=-3) to (4\ V \ @0.2\ V)</td>
<td>(V_{bs}=0) to (2\ V \ @1\ V)</td>
<td>(V_{ds}=0\ V)</td>
</tr>
<tr>
<td>Cgd</td>
<td>(V_{ds}=0) to (3\ V \ @0.2\ V)</td>
<td>(V_{gs}=0) to (3\ V \ @1\ V)</td>
<td>(V_{bs}=0\ V)</td>
</tr>
<tr>
<td>Cgs</td>
<td>(V_{ds}=0) to (3\ V \ @0.2\ V)</td>
<td>(V_{gs}=0) to (3\ V \ @1\ V)</td>
<td>(V_{bs}=0\ V)</td>
</tr>
<tr>
<td>Cgg</td>
<td>(V_{gs}=-3) to (3\ V \ @0.2\ V)</td>
<td>(V_{ds}=0\ V)</td>
<td>(V_{bs}=0\ V)</td>
</tr>
</tbody>
</table>

made for the accuracy between Id-Vd and Rout-Vd. The accuracy of C-V model are acceptable but the error here will impose a lower bound for the accuracy of RF circuit simulation.

The noticeable discrepancy between the capacitance data and the extracted model is the gate to body capacitance when the channel is turned on. The gate to body capacitance does not vanish to zero in BSIM3V3 while this problem does not appear in other SPICE model using Meyer capacitor model.
FIGURE 6. DC model extraction results from BSIMPro.
FIGURE 7. Capacitance model extraction results from BSIMPro.
2.3 *Non-Quasi-Static (NQS) effect of MOS transistor*

It is known that the transistor terminal charge will not follow the terminal voltage instantaneously. For example, when gate to source voltage increases, inversion charge will also increase. The additional charge can come from the source, drain and even the substrate. However, due to the non-zero channel resistance (Fig. 8), charge take time for travelling. This delay time is insignificant for low frequency application but will introduce noticeable magnitude and phase error for high frequency simulation.

*FIGURE 8. Distributive gate RC model.*
The channel of the MOS can be viewed as a bias dependent distributed RC network. In the BSIM3V3 NQS model, this is modeled as a single RC network with the RC delay equals the mean of the impulse response [3]. The model has a parameter ELM which can be used to tune the channel resistance.

2.3.1 Analysis of NQS effect in terms of Y-parameters

Fig. 9 show the Y-parameters of a 0.35um NMOS transistor in saturation region. Both source and substrate are connected to the ground. The Y-parameters are plotted from 1 to 26GHz and are normalized to corresponding low frequency QS model elements for easy comparison.

It is clearly shown that the QS model elements are constant and independent of frequency. On the other hand, both MEDICI simulation and BSIM3V3 NQS model show similar frequency dependent properties.

The difference between MEDICI simulation results and BSIM3V3 model at low frequency are the inherent error of the model extraction at the bias point. The overall error across different bias conditions are shown in Figs. 6 and 7 during model extraction.
The Ygg is the input admittance when the output is AC grounded. The error in Ygg is the major contribution to the incorrect input impedance prediction. Impedance matching is required to provide a stable RF circuit. For the application of low noise amplifier, we cannot
use the wide band lossy matching network (Figs. 2a and 2b on page 4) when noise performance is of concern. However, the narrow band lossless matching network (Fig. 2d on page 4) is sensitive to device parameters. BSIM3V3 model of Ydd shows largest error among the four parameters. This is mainly due to the difficulty of modeling output resistance and the missing model element of substrate resistance which is connected to the drain-body p-n junction. The inability of modelling the frequency depending small-signal model elements due to the NQS effect, not only gives deviated circuit design, but also leads to sub-optimal circuit architecture.

2.3.2 Impact of NQS effect on LNA architecture and performance

As mentioned before, source-inductive degeneration architecture is preferred by LNA circuit designer. Under quasi-static assumption and ignoring the presence of Cgd, the input impedance of the LNA in Fig. 10 is given by

$$Z_{in} = s(L_s + L_k) + \frac{1}{sC_{gs}} + \left(\frac{S_{m1}}{C_{gs}}\right) L_s$$ (Eq 2)

The impedance matching condition is fulfilled at the operating frequency $\omega_0$ when

$$\omega_0 = \frac{1}{\sqrt{(L_s + L_k)C_{gs}}} \quad \text{and}$$ (Eq 3)
Non-Quasi-Static (NQS) effect of MOS transistor

\[
\left( \frac{g_m}{C_{gs}} \right) L_s = Z_o = 50\Omega \tag{EQ 4}
\]

Where \(Z_o\) is the characteristic impedance of the system and is \(50\Omega\) in general.

From the above equations, we can see that the real input impedance is provided by the source inductor. This is the only way to provide a real impedance from reactive component but with the sacrifice of amplifier gain.

However, from both MEDICI simulation and device measurement (refers to Chapter 3), we will see that \(Z_{in}\) is not purely imaginary even though \(L_s\) is zero.

The real part and imaginary part of the input impedance of the NMOS are plotted in Fig. 11 and Fig. 12 respectively. The drain of the transistor is AC shorted to ground in order to
Non-Quasi-Static (NQS) effect of MOS transistor

**FIGURE 11.** The real part R of input impedance of transistor M1 when drain is AC shorted to ground.

**FIGURE 12.** Input capacitance C of the transistor M1 when the drain is AC grounded.
eliminate the impedance due to the output load seen through the capacitor Cgd. The equivalent small signal model of the input impedance is shown in Fig. 13. As shown in Fig. 11, with QS, the real part of the input impedance is zero, and this is the reason that leads to source-inductive degeneration matching technique employed in [2]. The real input impedance shown in both the BSIM3V3 NQS model and the MEDICI stems from the finite channel resistance that gets more significant as frequency increase. We can see from the Smith Chart in Fig. 14, the magnitude of S11 decreases and deviates from QS model more as frequency increases. The BSIM3V3 NQS model fits better than the QS model since it models the channel resistance by a first order RC network. Notice that, in Fig. 12, the capacitance of BSIM3V3 NQS model and QS model are different even at low frequency. This discrepancy may probably due to model implementation error. The error of the extracted capacitance (Cgs+Cgd) is less than 2.5% under this bias condition.
Setting BSIM3V3 NQS mode parameter ELM to 6 seems to model the real input impedance more accurately than the default value of 5. The ELM value of 3 was originally derived from channel charge in linear region, and the default value is a compromise between linear and saturation region. However, ELM equals 6 may not be a correct choice below 5GHz as seen in Fig. 15.

Once we realized that the simple common-source architecture can also provide a real impedance component for input impedance matching, a common-source architecture is
proposed for LNA design instead of source-inductive degeneration architecture due to the following reasons:

- the argument of using source inductor is invalid once we consider NQS effect of MOS transistor,
- one or two inductors can be eliminated in the case where the source inductor must be realized by on-chip inductor, e.g. differential LNA,
- amplifier gain is increased due to the absence of source degeneration,
- substrate parasitic connected to the source are shielded by grounded source node,

The comparison of LNA performance using MEDICI simulation, BSIM3V3 NQS model and QS model are shown in Figs. 16-21. The simulation results are also summarized in

![Figure 15](image.png)

**FIGURE 15.** The real part of input impedance of the cascode LNA without matching components. Below about 5GHz, BSIM3V3 NQS model of ELM equals 5 matches to MEDICI slightly better than that of ELM equals 6.
Table IV. The LNA is supposed to be operated at 2.4GHz and the gain increases as source inductance decreases.

**FIGURE 16.** Input match and gain of a 2.4GHz LNA using the source-inductive degeneration architecture and simulated with BSIM3V3 QS model. The result is compared against the MEDICI circuit-mode simulation.

**FIGURE 17.** $S_{11}$ and $S_{21}$ of the LNA in Fig. 16. QS model under-estimates the real input impedance. The $\star$ denotes the S-parameters at 2.4GHz.
FIGURE 18. Common-source matched 2.4GHz LNA using BSIM3V3 NQS model. The matching network can be a lump LC network or transmission line. This LNA gives highest gain because of no source degeneration.

FIGURE 19. S\(_{11}\) and S\(_{21}\) of the LNA in Fig. 18. Impedance mismatch shown from MEDICI S\(_{11}\) is dominated by the capacitance error of BSIM3V3 model. The matched frequency is shifted to 2.35GHz. The * denotes the S-parameters at 2.4GHz.
Non-Quasi-Static (NQS) effect of MOS transistor

**FIGURE 20.** Source-inductive degeneration matched 2.4GHz LNA using BSIM3V3 NQS model. The source inductor is smaller than that using QS model for simulation. The gain of the LNA increases as a result of reduced source degeneration effect.

**FIGURE 21.** $S_{11}$ and $S_{21}$ of the LNA in Fig. 20. The matched frequency is also shifted to 2.35GHz. The $\star$ denotes the S-parameters at 2.4GHz.
TABLE IV. Summary of LNA designs using BSIM3V3 NQS and QS model.

<table>
<thead>
<tr>
<th></th>
<th>Common-source matched using NQS model</th>
<th>Source-inductive degeneration matched using NQS model</th>
<th>Source-inductive degeneration matched using QS model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source inductor</td>
<td>0 nH</td>
<td>0.44 nH</td>
<td>1.17 nH</td>
</tr>
<tr>
<td>Gain from SPICE at 2.4GHz</td>
<td>8.0 dB</td>
<td>6.0 dB</td>
<td>5.0 dB</td>
</tr>
<tr>
<td>Maximum gain from MEDICI at resonant frequency</td>
<td>5.9 dB at 2.35GHz</td>
<td>5.0 dB at 2.35GHz</td>
<td>3.3 dB at 2.4GHz</td>
</tr>
</tbody>
</table>

2.4 Summary

The high frequency characteristics of MOS device are studied through both MEDICI device simulation and SPICE simulation using BSIM3V3 model. Ignoring NQS effect not only results inaccurate simulation but also non-optimized RF circuit design. BSIM3V3 NQS model is recommended for SPICE simulation for RF circuit design but limitation of the model accuracy has to be bared in mind.
CHAPTER 3

Device Characterisation of 0.35µm CMOS devices

3.1 Introduction

To understand the device characteristic and explore the feasibility of 0.35µm CMOS technology for 2.4GHz RF circuit application, a 50µm wide NMOS testing device was fabricated using HP 0.35µm process. The test device was intended for microwave frequency characterisation using a Vector Network Analyser.

3.2 Layout consideration

MOS transistors are 4-terminal devices. Their small-signal characteristic can be completely represented by a 3-port network parameter matrix. Most vector network analyser
can measures up to 2-port network parameter. 3-port measurement can be realized by measuring 2 of 3 ports in turns and terminating the remaining port by a broadband 50Ω load. Since the purpose of fabricating the testing device in our case is to find out the cut-off frequency of the 0.35um CMOS technology and that the critical transistor of the LNA to be designed is using common-source configuration, the NMOS transistor was laid out in the 2-port configuration with both source and substrate connected to the ground pads as shown in Fig. 22. For such small size of transistor, parasitic capacitance of probing pads and connecting wire are comparable to the intrinsic capacitance of the device. A dummy device was also laid out for de-embedding [9] as shown in Fig. 23.
3.3 Measurement and comparison to BSIM3V3 model

The testing device was fabricated through MOSIS in 4 metal layers, n-well and 0.35um feature size HP GMOS10QA process. The die photo of the testing device is shown in Fig. 24. In addition to our extracted BSIM3V3 model, MOSIS for the first time also provides the BSIM3V3 model. So all measurement results are compared with SPICE simulation using these models and see how much deviation. These results give us a clue as to where we should pay attention when we use this model for next circuit design using 0.35um technology.
3.3.1 DC characteristic

Fig. 25 shows the Id-Vg curves and Fig. 26 shows the corresponding gm-Vg curves. The r.m.s. errors are 27% and 28% respectively. Fig. 27 shows the Id-Vd curves and Fig. 28 shows the corresponding Rout-Vd curves. The r.m.s. errors are 10% and 9% respectively.

3.3.2 AC characteristic

The cut-off frequency \( f_c \) of a 2-port active device (Fig. 29) is the frequency where the current gain is unity, i.e.

\[
i_o = i_i \quad \text{or} \quad H_{21} = \frac{i_o}{i_i} = 1 \quad \text{at} \quad f_c
\]

\[(\text{EQ 5})\]
FIGURE 25. Id-Vg of NMOS testing device.

FIGURE 26. gm-Vg of NMOS testing device.
FIGURE 27. Id-Vd of NMOS testing device.

FIGURE 28. Rout-Vd of NMOS testing device.
The H21 of the transistor is plotted in Fig. 30 and the cut-off frequency is 10 GHz. The NQS model shows over-estimated cut-off frequency compared to QS model. The difference can be attributed to the reduced input capacitance and the additional channel resistance in NQS model. These two effects reduce the input AC current and hence increase the current.
gain. The real and imaginary parts of input impedance after de-embedding are plotted in Figs. 31 and 32 respectively. The measurement results show similar trend as the MEDICI simulation results shown in Figs. 11 and 12 on page 21. However, the real part of the input impedance as a few ohms higher than the NQS model simulation. The extra resistance is partially due to the gate-poly resistance even fingering technique was used.
3.4 Summary

The cut-off frequency of the 0.35um NMOS transistor is around 10GHz as shown from both measurement and BSIM3V3 model simulation. It is concluded that 0.35um device has potential for 2.4GHz RF circuit application. The BSIM3V3 NQS model shows agreement with measurement results with less than 5% discrepancy. It is highly recommended to use NQS model of BSIM3V3 for RF circuit simulation.
CHAPTER 4

A 2.4GHz Single-ended LNA

4.1 Introduction

Due to the existence of NQS effect, the reason of using source-inductive degeneration matching technique turns out to be redundant. Source-inductive degeneration results in undesirable amplifier gain reduction. As an illustration, a cascode common-source amplifier for 1.5-volt power supply application was fabricated using HP 0.35um process. The amplifier was externally impedance matched for optimal noise and gain performance at 2.44GHz. Various circuit performances were then measured. The LNA is supposed to be used for 2.4GHz ISM band application using Spread-spectrum. The available frequency range is from 2.4GHz to 2.483GHz and the LNA is tuned at the center of the frequency band.
4.2 Design and layout consideration

A schematic of the LNA is shown in Fig. 33. The size of the input transistor M1 is 50μm by 0.4μm. It is chosen such that the required Q-factor of the input match network is reasonable but still can support enough amplifier gain. The size of the cascode transistor is 630μm by 0.4μm which can provides large transconductance for low impedance path. The gate of the transistor M2 is shunted to ground by a large MOS capacitor to absorb any noise from the power supply.

The entire circuit including bonding pads occupies 0.87x0.58 mm² chip area. Four pads were allocated to the source node of the transistor M1 and another three pads for the substrate contact in order to reduce parasitic bonding wire inductance. The input matching network is realized externally instead of on-chip. In our intended application, the LNA will be connected...
immediately after the antenna, and the antenna will provide some filtering and the required source impedance. Same argument also applies to the output matching network. The output of the LNA will be connected to the next stage on-chip amplifier or mixer and hence, 50-ohm matching is not required. However, for the circuit testing purpose, both input and output of the LNA are matched externally to 50Ω impedance of the measurement equipment.

To reduce the gate-poly parasitic resistance which will degrade the gain and noise performance, interdigitation was used to cut the poly resistor into small pieces and connected them in parallel from both ends.
4.3 Test set-up

The die photo of the LNA is shown in Fig. 34. The die was mounted on a PCB using conductive epoxy for proper backside contact. Both input and output matching networks, as shown in Fig. 35, were implemented by microstrip lines.

FIGURE 34. Die photo of the single-ended LNA. Input at left and output at right.

FIGURE 35. The impedance matching networks implemented by microstrip lines.
S-parameter was measured using a HP8510C Network Analyzer while noise performance was observed with a HP8970B Noise Figure Meter. For the linearity measurement, input signals were supplied from a HP E4122B and a HP 83752A signal generators and were combined together, in the case of two-tone test, by Mini-Circuits ZFSC-2-2500 power combiner. Output signal level was measured with a HP8563E Spectrum Analyzer. The LNA was biased through bias-T. The LNA was designed for 1.5 volt power supply but lower supply voltage were also used for S-parameter and noise measurements.

4.4 Measurement results

4.4.1 Amplifier gain, matching and reverse isolation

The amplifier gain, input and output matching and reverse isolation of the LNA were measured in terms of S-parameters by network analyzer. The influence of bias-Ts were taken care by the build-in calibration procedure of the network analyzer. The loss of the connecting microstrip lines, shown in Fig. 36, were accounted for actual amplifier gain by compensating the through line loss as shown in Fig. 37.
Fig. 38 shows the forward gain of the LNA which peaks around 2.39GHz and has a 150MHz 3dB bandwidth. The maximum gain achieved was around 7dB with about 3.66mW DC power dissipation.

The input and output matching were measured by its reflection coefficients S11 and S22. A -10dB reflection coefficient suggests an acceptable level for 50Ω impedance matching. The reverse isolation was measured by backward transmission coefficient S12. The smaller the value, the better the isolation. Figs. 39-41 show the measured S11, S22 and S12 respectively.
In the case where 50Ω impedance matching is not a constrain, 10dB gain can be achieved with same noise performance and -2.5dB and -4.7dB for input and output reflection coefficients respectively.

4.4.2 Noise figure measurement

The testing set-up is shown in Fig. 42. The noise figure and loss of components between the noise source and the input of the LNA were measured separately. The actual noise figure $F_3$ of the LNA was then calculated from

$$F_{cas} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots$$  \hspace{1cm} (EQ 6)

FIGURE 40. Output match, S22.
FIGURE 41. Reverse isolation, S12.

FIGURE 42. Noise measurement set-up.

Because of the high amplifier gain, the noise figures of components connected after the LNA can be ignored. The noise figures of the LNA for different power supply is shown in Fig. 43.
4.4.3 Large signal linearity

The amplifier will get saturated after a certain input power. This large signal linearity is measured by output 1dB compression point. This value set the upper bound of the dynamic range of the LNA as shown in Fig. 44.
The output power of the LNA was measured at 2.39GHz with 1.5V power supply. Fig. 45 shows the output power versus the input power of the LNA. The output power of 1dB compression point is shown to be -14dBm.

Use the noise figure of the LNA and output noise power equation

\[ N_o = GFkT_0B \]  

(EQ 7)
The lower bound of the dynamic range $N_0$ is found to be -83dBm for 83MHz bandwidth of 2.4GHz ISM band and so the dynamic range is 69dB.

4.4.4 Small signal linearity

The small signal linearity of the LNA was measured by its two-tone intercept point IP3. Two closely spaced equal amplitude input signals at 2.385GHz and 2.395GHz were applied to the LNA through power combiner. The intermodulation products of the two signals lied at 2.375GHz and 2.405GHz as shown in Fig. 46.
Fig. 46. Power spectrum of LNA output when two tones applied to the LNA input (2.385 and 2.395GHz). The two other signals were the intermodulation products (2.375 and 2.405GHz).

Fig. 47 shows the fundamental and third intermodulation product at the output versus the input power. The IP3 is shown to be -3.7dBm at the output.
4.5 Summary

The performance of the LNA is summarized in the Table V. The noise figure of the LNA is low enough for usual LNA application. Since there is no published LNA implementation using CMOS at 2.4GHz, no comparison can be done at this stage. More researches are needed to find a optimal transistor size for better noise performance.
**TABLE V. Summary of the LNA performance.**

<table>
<thead>
<tr>
<th>VDD</th>
<th>1.5V</th>
<th>$S_{22}$</th>
<th>-1.1dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{dc}$</td>
<td>3.66mW</td>
<td>NF</td>
<td>4.8dB</td>
</tr>
<tr>
<td>$f_0$</td>
<td>2.39GHz</td>
<td>1dB CP, output</td>
<td>-14dBm</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>-8.54dB</td>
<td>IP3, output</td>
<td>-3.7dBm</td>
</tr>
<tr>
<td>$S_{21}$</td>
<td>7dB</td>
<td>dynamic range</td>
<td>69dB</td>
</tr>
<tr>
<td>$S_{12}$</td>
<td>-16.3dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Sub-micron CMOS device characteristics have be studied using 2-D device simulation program. BSIM3V3 model is widely used for sub-micron device simulation due to its excellent scalability. The ability of BSIM3V3 model to predict high frequency characteristic of MOS transistor was studied by comparing to device simulation results. BSIM3V3 NQS model will improve the simulation accuracy especially for gate input impedance prediction. Different LNA design architectures were revised and found that the source-inductive degeneration matching technique, used by some engineers, use quasi-static assumption. The improper assumption for microwave frequency circuit design turns out to be sub-optimal. Simple common-source configuration can also fulfil the impedance matching requirement.
without using lossy component. It was shown that this configuration give better circuit performance using both device simulation program and BSIM3V3 NQS model.

Base on the above analysis, a 1.5 volt 2.4GHz LNA using 0.35μm CMOS technology was designed and fabricated. Circuit performance was measured to investigate the possibility of using CMOS technology for 2.4GHz RF circuit application. The LNA worked quite well except the substantial high noise figure. The high noise may due to inherent CMOS properties but currently there is no published result for comparison. The LNA is very suitable for 1.5V battery supply application.
References


