Characterization and Reduction of Thermal Boundary Resistance of CVD-Graphene Interfaces

By

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This is to certify that I have examined the above MPhil thesis and have found that it is complete and satisfactory in all respects, and that any and all revisions required by the thesis examination committee have been made.

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Abstract

With development of nano-fabrication technology, feature size and dimension of microelectronics are approaching nanoscale. A phenomenon of this size-shrinking trend is that the properties of interfaces between contacting materials are becoming dominant factors affecting performance of microelectronics. Researchers have devoted countless efforts to investigate properties of materials at nanoscale, but knowledge about the interfaces is still insufficient. Graphene is considered as one of the miracle materials for next generation microelectronics due to its two-dimensional nature. The extraordinary high thermal conductivity and electron mobility of graphene attract researchers to integrate graphene into microelectronic devices. However, since graphene is just an atomic structure of one or a few atom layers, the interfaces between graphene and another kind of material strongly influence the performance of graphene based devices. This research selects thermal boundary resistance of graphene interfaces as the topic, which is very important for the thermal management in graphene microelectronics and even for the feasibility evaluation for other potential graphene applications. By the implementation of 3ω method, thermal boundary resistance, which is the basic index to evaluate thermal transport of interfaces, of several kinds of graphene interfaces is characterized, to evaluate thermal transport of the interfaces. The effects of interfacial interaction on the thermal boundary resistance are further explored. The formation of well-adhesive interfaces is of great importance to realize graphene microelectronics. On the other hand, covalent bonds between the carbon atoms of graphene and the atoms of another contacting material assist the heat transfer across interfaces.
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CHAPTER 1
INTRODUCTION

1.1 Thermal Boundary Resistance

1.1.1 Definition

Thermal boundary resistance (TBR), or Kapitza resistance in some literature to acknowledge the person who first quantificational discovered this property, is a kind of thermal resistance creating a temperature discontinuity at an interface between two materials in intimate contact when heat is transferred across the interface. So the thermal boundary resistance of an interface is defined as the temperature discontinuity at the interface divided by the heat flux flowing across the interface.

\[ R_{th} = \frac{\Delta T}{J} \]  

(1.1)

Where \( \Delta T \) is the temperature discontinuity, \( J \) is the heat flux and \( R_{th} \) is the thermal boundary resistance with unit K·m\(^2\)/W. This thermal transport phenomenon seems similar to thermal contact resistance which also describes a temperature discontinuity at the interface between two contacting solids, but the difference of their applicable scale makes these two terms inherently unequal. Thermal contact resistance is related to poor mechanical connection between two solids, while thermal boundary resistance is related to the abrupt disordered of atoms and the dissimilarity in the intrinsic nature of materials.

Thermal contact resistance is used to describe the thermal transport phenomena in macro scale. A temperature discontinuity is observed between two contacting solids surfaces because the two surfaces actually contact to each other only at a few discrete locations rather than over the entire surfaces. Such discretion results from the microscopically visible voids or pitches of the two surfaces. Thermal contact resistance is influenced by the contact pressures which can cause deformation of the surfaces, interstitial materials which can fill the gaps between the surfaces, and surface properties such as cleanliness and roughness. A method to handle thermal contact resistance is the application of thermal interface materials (TIM). Thermal interface materials are used to bond two surfaces together and enhance thermal dissipation from the hot side to the cool side at the same time. TIMs fill voids and gaps between two surfaces, creating more efficient heat dissipation paths. Generally, TIMs are made from
polymers which always have a very low thermal conductivity, so polymer composites with nano-fillers are widely utilized because they contain fillers which enhance thermal conductivity. However, the overall thermal conductivity of the composites is not only determined by the intrinsic thermal conductivities of polymer matrixes and fillers, but also highly affected by the percolation of fillers and interfaces between matrixes and fillers. The manipulation of the later factor to improve the performance of composites requires reduction of thermal boundary resistance of the interfaces. This demonstrates the difference between thermal contact resistance and thermal boundary resistance in terms of their application scales.

Thermal boundary resistance is used at nanoscale. A small temperature discontinuity can still be observed even at a perfectly and intimately atomic interface. This phenomenon was first detected by Kapitza through an experiment on the interface between copper and superfluid helium. Later, Swartz and Pohl gave a comprehensive review on thermal boundary resistance in 1988, including the summaries of both theories and experiments on fluid/solid and solid/solid interfaces [1]. They considered the differences of energy carriers of two sides and the disruptions of carriers propagation paths from one side to another the two main factors contributing the existence of thermal boundary resistance. They suggest that the thermal boundary resistance is not fully understood. The contribution to thermal boundary resistance are not only materials discontinuities at interface, but also disordered regions near interface.

![Image of two kinds of thermal resistance](image)

**Fig. 1.1** Illustration of two kinds of thermal resistance, thermal contact resistance (left) and thermal boundary resistance (right).

Academia and industry both demand further understanding of thermal boundary resistance. Microelectronics is one of the fastest-growing industries seeking development
based on knowledge of thermal boundary resistance. As the development of the microelectronics industry is towards thinner, smaller and more integrated devices, their sizes have reached down to nanoscale, and the structure of these devices has been transformed from single to multilayers. As a result, the materials of devices have become less bulky, with more and more interfaces existing inside these devices. The properties of the interfaces are beginning to determine the performance of the devices. From the thermal aspect, the interfaces will serve as an additional thermal resistance to obstruct heat dissipation. Regarding joule heat dissipation issues in microelectronics systems, thermal boundary resistance of the interfaces is of great importance to evaluate the performance of new devices and interfaces with poor thermal conductance will degrade the performance of these devices. However, in some applications thermal boundary resistance will enhance their performance. In other applications such as those for reserving heat, e.g. thermal barrier coatings, such interfaces help to increase the performance because the interfaces serve as disorder zones to isolate heat and prevent it from dissipating. So there is a strong demand to understand thermal boundary resistance and this knowledge can lead to breakthroughs in these applications. To give a clear picture of the effect of thermal boundary resistance, a simple calculation can be used as an example. The typical quantity range of the thermal boundary resistance of a metal/dielectric interface is from around $10^{-7}$ to $10^{-9}$ K·m$^2$/W [2] and the thermal conductivity of a common dielectric material, silicon oxide, is around 1 W/m·K. Based on the thermal resistance $R_{th}$ calculation equation for a specific solid,

$$ R_{th} = \frac{t}{k} $$

(1.2)

where $t$ is thickness and $k$ is thermal conductivity, we can obtain the equivalent silicon oxide thickness of the typical thermal boundary resistance of a metal/dielectric interface which is around 5nm to 100nm. This is quite significant when the feature size of microelectronics is approaching tens of nanometers.

Due to advances in nanofabrication technology and development of precise detection instruments, observation of this phenomenon becomes possible. Thus, characterization and manipulation of thermal boundary resistance have attracted attentions, especially from those in the microelectronics industry. With discoveries of more reliable correlations between temperature of materials and precise models of heat dissipation inside a complex structure, even a small response from thermal boundary resistance can be extracted. This development
will contribute to the active thermal management of microelectronics, e.g., improving heat dissipation by lowering thermal boundary resistance. Furthermore, through a combination of advanced materials characterization techniques, we can relate the variation in thermal boundary resistance to the atomic structures of interfaces. This facilitates the discovery of the principles of nanoscale heat transfer and would generate more insightful ideas on this fields [3].

The concept of thermal boundary conductance is also widely used to describe this property, which is the inverse of thermal boundary resistance. The conversion may be omitted in the rest of the thesis.

\[ h_{BD} = \frac{1}{R_{th}} \]  

(1.3)

1.1.2 Theory of thermal boundary resistance

Thermal boundary resistance is caused by the discontinuities at interface which disrupts the regularity of thermal transport patterns. There are mainly three factors defining the thermal transport pattern, i.e., types of heat carriers, dissimilarity of two materials on each side, and energy exchange mode of an interface [1].

Electrons and phonons are the two main kinds of heat carriers. In a metal, there is a very large concentration of free roaming electrons, and these electrons do not just carry charges to generate electrical conduction, they also transport heat. But in electrical insulators or semiconductors, electrons are either fixed by the atomic bonds or only a small amount is intentionally excited, so the heat carried by the electrons can be neglected. Dominant heat carriers become phonons which represent the vibration of atoms in materials. This vibration generates thermal waves and propagates inside material structures to transport heat. When the electrons act as the dominant heat carriers across the interface, like a metal/metal interface, the thermal boundary resistance is much lower than the case in which the phonons take the responsibility of transferring heat across an interface, i.e. dielectric/dielectric or metal/dielectric interface. Electrons dominated interfaces are more convenient and easier to predict by theoretical models when compared with phonon dominating interfaces. Thus, most of the effort has been focused on understanding the later. In theory, depending on the definition of the interface and the mismatch of the phonon properties which determine the
transmission of phonon energy, there are two basic models for predicting thermal boundary resistance, i.e., the acoustic mismatch model (AMM) and diffusive mismatch model (DMM).

In the acoustic mismatch model, an interface is treated as a flat plane without any effect on incident phonons, and the mismatch of the materials is represented by acoustic impedance mismatch. Acoustic impedance $Z$ is defined as the product of density $\rho$ and the speed of sound $v$ of phonons.

$$Z = \rho v$$  \hspace{1cm} (1.4)

Then the acoustic impedances of two materials capture the transmission coefficient of phonons.

$$t_{AB} = \frac{4Z_A Z_B}{(Z_A + Z_B)^2}$$  \hspace{1cm} (1.5)

Once the transmission coefficient is obtained, it can be combined with other models, such as isotropic Debye solid, to describe the phonon properties of materials and to calculate the thermal boundary resistance. But this model fails completely in the case of twin grain boundary, which results in a 100% transmission. This failure is caused by the neglecting of the interface properties.

To overcome this disability, a diffusive mismatch model is proposed. In the diffusive mismatch model, an interface refreshes the incident phonons, which means the phonons hitting the interface lose the memory of the side they come from. This implies that the transmission coefficient depends on the ratio of the phonon density of states in a material. Also in the diffusive mismatch model, diffusive scattering indicates scattering is elastic and thus the frequencies of the phonons do not change during scattering. The equations of the diffusive mismatch model are more complex and not shown here, but they are the same as those of the acoustic mismatch model. They provide the transmission coefficient of an individual phonon to calculate the thermal boundary resistance by the summation of all phonons.

While both AMM and DMM provide values for thermal boundary resistance, they calculate them purely based on the bulk properties of the two materials forming an interface; thus they do not account for the actual complexity of real interfaces, including such parameters as interfacial bonding strength, roughness and defects. Molecular dynamic (MD)
simulation is one of the prominent approaches that can take the complex properties of interfaces into account [4] to calculate thermal boundary resistance. In MD simulation, atoms and molecules follow the classic dynamics based on the solution of Newton’s second law of motion. So, the description of the forces between atoms and molecules is the essence in simulation. The forces can be derived from the interatomic potential which varies with the atomic structure and the environment surrounding the atoms. By the atomic scale simulation approach i.e. the first principle method to calculate the potentials of the structures varying with defects and bonds, or deriving the potentials from well-implemented experiments, the MD simulation can calculate the thermal boundary resistance of interfaces with complex structures. As methods for theoretical prediction are still being developed to explain the atomic systems with unavoidable imperfections and complex states of interactions, there is a demand for direct experimental studies on thermal boundary resistance to provide ideas to better understand the effects of defects, bonds and other imperfections. Furthermore, guidelines and methods for handling this property can also be explored through the experimental studies. In this work, we focus on the experimental studies on thermal boundary resistance. Characterization techniques on this property will be discussed in subsequent sections.

1.1.3 Factors affecting thermal boundary resistance

From a previous discussion, we have learned that thermal boundary resistance is determined not only by the nature of materials but also the characteristics of interfaces. As the nature of materials is hard to modify, to explore the correlation between thermal boundary resistance and the characteristics of interfaces becomes a more plausible way to manipulate thermal boundary resistance. Different from a perfect interface which is flat and uniform, a real interface usually contains atomic imperfections, i.e. compositional intermixing, roughness, and covalent bonds. These imperfections generally increase the disorder of an interface, but the mechanism through which energy is transported across the disorder is not clear yet. Researchers can only learn from some the summary of trends from the limited experimental studies on the relationship between thermal boundary resistance and interfacial disorder [6].

When compositional intermixing happens in an interface, the interface transforms from an abrupt compositional separated plane to a thin layer of mixing region of two materials. The mixing region may form an alloy of the two materials and even an amorphous zone. Such intermixture may increase the phonon scattering times and thus decrease the efficiency of
phonon energy transfer. An obvious trend is that the appearance of compositional intermixing will increase thermal boundary resistance [7].

The roughness of interface means that the interface loses its flatness but still keeps the compositional separation. An observation of the phenomenon between the RMS of the roughness of an interface and the thermal boundary resistance of the interface indicates that the larger the RMS of roughness, the larger the thermal boundary resistance. The roughness may decrease the phonon transmission coefficient, which is supported by the hypothesis that the roughness will absorb the phonons with a wavelength shorter than the size of roughness [8].

The covalent bonds have a positive effect on thermal transfer across an interface, which means thermal boundary resistance will be decreased by the stronger interfacial bonding. One theory to explain this phenomenon is that the interfacial bonding will increase the stiffness of the interface, which initially decreases the thermal boundary resistance, but the mechanism for this easily observed phenomenon is not conclusive. However, manipulating the interfacial bonding strength is still believed to be one useful way to tune thermal boundary resistance [9, 10].

1.1.4 Measurement techniques for thermal boundary resistance

To measure the thermal boundary resistance, the biggest challenge is the quantification of the temperature discontinuity across the measured interface because it is too small to detect by common temperature sensing methods. Thus, a general principle to obtain thermal boundary resistance depends on the extraction of the thermal boundary resistance from a heat transport model of which the total temperature variations is relatively easy to characterize. The time domain thermoreflectance (TDTR) technique and the 3ω method are two measurement techniques that follow this principle for measuring thermal boundary resistance. The 3ω method is employed in this work. Therefore, a brief introduction to TDTR is given here, and a detailed explanation of the 3ω method will be presented in the next chapter.

The TDTR technique is one of the most powerful thermophysical property characterization techniques by applying the advancement of high frequency laser. This technique was originally developed by Paddock and Eesley, and Capinski and his coworkers. Later, Cahill modified the technique to improve its accuracy. In short, the TDTR is a pump-
probe method where laser radiation from a pump beam is used to heat the sample and the decay of the surface temperature is measured using a time delayed probe laser beam [3].

![Diagram of hardware setup of time domain thermoreflectance](image)

**Fig. 1.2** Illustration of the hardware setup of time domain thermoreflectance [4].

The technique takes advantage of the fact that the reflectivity of metal to some extent depends on temperature. For a small temperature rise, reflectivity is linearly proportional to the temperature rise. So a thin metal layer is applied as a transducer to sense the temperature rise of a sample surface heated by a laser, for example, a thin layer of Al (80nm~100nm) is deposited on the surface of the sample. A pump heat pulse is focused on the sample and the laser energy is absorbed by the metal layer. Then the temperature of the metal film decays as the heat diffuses through the underlying layers and interfaces after energy is redistributed which is a quantified time stamp of the metal transducer. A time delayed probe beam is then focused on the same spot of the sample, and the change in the reflectivity of the Al film is measured using a photodiode detector and lock-in amplifier. This change in reflectivity is related to the surface temperature, thus the temporal decay of surface temperature is measured. The experimental data is fitted to the heat transport model for layered geometries by adjusting the unknown free parameters. Such free parameters are the thermal conductivities of materials and the thermal boundary conductance of interfaces.

Over the past decades, the TDTR has been applied across the entire range of cross-plane thermal conductivity measurement, from the high thermal conductivities of diamond and metals to the ultralow thermal conductivities of disordered layered crystals and fullerene derivatives [4]. Essentially the same method can be applied to bulk materials, thin layers, and individual interfaces with both high (e.g., TiN/MgO and Al/Cu) and low (e.g., Bi/H-
terminated diamond) levels of thermal conductance [5]. A summary of the measurement results by TDTR is shown in Fig. 1.3. According to Fig. 1.3, thermal boundary resistance (inverse of the thermal boundary conductance in Fig. 1.3) spans a relatively modest range (~100×). The electron mediating thermal transport gives an interface a small thermal boundary resistance. Due to the similarity in phonon properties and the low mismatch of the lattice structure, the TiN/MgO interface shows a low thermal boundary resistance even as the thermal transport is dominated by phonons. When these two parameters show a big difference, the thermal boundary resistance will increase considerably, such as that measured at the interface between the hydrogen-terminated diamond and Bi.

![Fig. 1.3 Thermal boundary conductance of various materials interfaces](image)

The two major advantages of the TDTR technique are: (i) it is a non-contact technique and requires little or even no sample preparation, and (ii) the technique quantitatively measures the thermal conductivity of materials and the thermal boundary resistance of interfaces simultaneously. Although the TDTR is the most popular and convenient way to measure thermal boundary resistance, it requires a sophisticated optical system which is quite expensive and installation time consuming. Thus, considering the cost and time to implement the measurement system, I choose the 3ω method, which is a less expensive and easier technique to setup.
1.1.5 Thermal boundary resistance of graphene interfaces

Graphene has been a promising material both in scientific research and microelectronic application since it was discovered in 2004 [11]. Its intrinsic 2D crystal structure offers many unique properties. Researchers have conducted many experiments to characterize the properties of graphene, especially high-quality graphene: room-temperature electron mobility of $2.5\times10^5$ cm$^2$/V·s; Young’s modulus of 1 TPa and intrinsic strength of 130 GPa; very high thermal conductivity; optical absorption of exactly $\pi\alpha<2.3\%$ (in the infrared limit, where $\alpha$ is the fine structure constant); complete impermeability to any gas; ability to sustain extremely high densities of electric current, a million times higher than copper. Another property of graphene already demonstrated is that it can be functionalized by chemical interaction. In terms of thermal aspects, according to some recent reviews, the intrinsic thermal conductivity of suspended graphene is normally above 2000 W/m·K and can reach as high as 5000 W/m·K [12-14], which is one order of magnitude higher than common thermal conductive metals. However, all of these reviews stress that when graphene is supported on a substrate or dispersed in a matrix, the intrinsic thermal conductivity of graphene will be suppressed greatly to as high as one order of magnitude lower by the interfacial interactions with other materials, which causes degradation of graphene and insufficient enhancement of graphene composites. Also they attribute the large variation in thermal conductivity measurement of graphene to the difficulty in the quantification of this suppression in different measurement setups. This phenomenon implies that the thermal transport of graphene is strongly affected by the interface between graphene and contacting materials. Seol et al suggest that the phonon leakage from graphene to a substrate may be the reason for the reduction of the thermal conductivity of graphene in their work which only gave 600 W/m·K for SiO$_2$ supported graphene [15]. However, in most applications graphene is always contacting with other materials; as a result, especially for thermal management in graphene microelectronics, to understand how heat is transported in the interfaces has become an eager issue to clarify in order to pave the road of excellent graphene devices. Furthermore, graphene has been used as a kind of fillers to enhance the performance of thermal interface materials or as a protective layer to protect the interconnect metal from degradation. All of these applications involve the thermal properties of which thermal boundary resistance is the most important of the interfaces. Therefore to characterize the thermal boundary resistance of graphene interfaces
attracts a large amount of interest not only to evaluate their application potential but also to develop a corresponding thermal transport theory.

Chen et al. measured the thermal boundary resistance between mechanically exfoliated graphene and silicon oxide by the 3ω method [16]. They sandwiched the graphene sheet between two layers of SiO₂, and assumed the two interfaces shared the same thermal boundary resistance. The results showed that the thermal boundary resistance varied from 5.6×10⁻⁹ to 1.2×10⁻⁸ K·m²/W, and this indicates that the DMM model fails to predict the thermal boundary resistance of the graphene/SiO₂ interface due to the amorphous nature of silicon oxide, the high anisotropy of graphene and the unclear phonons scattering in the graphene interface. Cai et al. fabricated a substrate with micro holes and transferred the CVD-graphene to the substrate. By employing laser heating and the relationship between graphene temperature and Raman spectral, they could determine the local temperature of the graphene [17]. Through carefully modeling the heat transport process, they obtained room-temperature thermal conductivity and interface conductance of (370 + 650/-320) W/(m·K) and (28 + 16/-9.2) MW/(m²·K) for the supported graphene. Later Schmidt et al. systematically studied the thermal boundary conductance of metal/graphite interfaces by TDTR [18]. The thermal boundary conductance ranged from 30 to 100 MW/(m²·K), which was 10⁻⁸~3×10⁻⁸ K·m² /W in terms of thermal boundary resistance. They also compared the experimental results with that predicted by the theoretical model, and explained the mismatch between experiment and theory as resulting from the interfacial mixing effect and metal-carbon adhesion forces, the stronger adhesion, and the higher thermal boundary conductance. Y. Koh et al. reported the thermal conductance of Au/Ti/exfoliated graphene/SiO₂ interfaces to be around 25 MW/(m²·K), and claimed that such a thermal conductance magnitude was the conductance of two serial thermal resistances of the Ti/graphene interface and graphene/SiO₂ interface by comparing their results to the summation of the Chen’s result and Schmitd’s result [19]. Pablo et al. presented results of a similar experiment to investigate the metal/CVD-graphene interface, which verified the former’s conclusion and proposed a correlation between the Debye temperature of metal and thermal boundary conductance [20]. He suggests that graphene has a better thermal contact with metals having a high Debye temperature.

Instead of focusing alone on thermal boundary resistance, some researchers also studied the material interaction of graphene interfaces, which intrinsically determine the thermal boundary resistance. Seung et al. investigated the interaction between graphene and different dielectrics [21]. They conclude that graphene tends to have a stronger interaction with the
dielectric of a higher dielectric constant, but the effects of the interaction strength on thermal boundary resistance is not revealed. Hopkins et al. demonstrates that the plasma-based functionalization of the graphene surface is a viable approach to manipulate the thermal boundary resistance between graphene and metal [9]. The oxygen absorbates on the functionalized graphene surface transformed the weak van der wards bonding of the metal/graphene interface to strong chemical bonding. These chemical bonds enhanced the thermal transport by influencing phonon flux and vibration mismatch. By applying laser annealing, Ermakov et al. observed a reduction in the thermal boundary resistance between graphene and substrates and conclude that the increased contact area and enhanced adhesion due to the local melting of the metal sub-layer are the reasons for the improvement [22]. From these researches, we learned that the thermal boundary resistance of graphene interfaces is a dominating factor of the heat dissipation in graphene devices; it is a drawback which limits the intrinsic thermal conductivity of graphene and may cut down the range of application of graphene. However, the thermal boundary resistance of the graphene interface is shown to be tunable. In other words, it is possible to control the thermal boundary resistance according to the requirements of a particular application. This is an area which requires more investigation.

1.2 Characterization of Graphene Interfaces

Through the above discussion, it should be established that characterization of graphene interfaces is the theme of this work. Exploring further on the real interfaces and providing more valuable information for applications are the objectives of this research.

1.2.1 Research motivation

Novoselov, one of the researchers who discovered graphene, has published a review as a roadmap for graphene research [23] in which they evaluated the existing directions of the application of graphene. Even though they admitted the material possesses excellent properties and high potential and praised it as a miracle material, they also expressed doubts about the weakness of graphene applications in the comparison with mature technologies. In the review, the chemical vapor deposition (CVD) graphene production method is touted as the most promising technology for mass fabrication of graphene. Therefore, CVD-graphene is selected as the graphene source in this research, which can simulate the real interfaces generated by feasible applications. Meanwhile, they stressed graphene microelectronics as a major direction, and in the high-frequency transistors section they proposed that the
dielectrics in contact with graphene be replaced by one having a higher dielectric constant. Following this advice, it was found that the high-\(\kappa\) aluminum oxide integrating with graphene had been demonstrated as a superior performance transistor [24-26]. But as Freitag et al. reported, energy dissipation must be considered carefully because the weak van-der-Waals connection between graphene and dielectrics enlarged the thermal boundary resistance [27]. Thus, it is worthwhile to investigate the thermal boundary resistance of the interface between CVD-graphene and aluminum oxide to supplement the knowledge from thermal transport aspects. Hopkins discussed several factors that affect thermal transport across solid interfaces. Intermixing, roughness, and bonding are common nanoscale imperfections that cause the real thermal boundary resistance to deviate from the theoretical value [6]. Another recent study shows that the electrical properties of graphene could be enhanced by annealing the graphene device and this is attributed to the formation of metal carbides on the interface [28, 29]. In other words, the bonding of the interfaces of graphene and specific metals can be strengthened by an annealing process, which may also be an approach to enhance thermal transport. As the discussion in the previous paragraphs section, tuning the thermal boundary resistance of graphene interfaces is possible and significant.

1.2.2 Research objectives

Characterization of the thermal boundary resistance and elucidating the effects of annealing on thermal boundary resistance are the objectives of this research. The 3\(\omega\) method is selected as the measurement technique and an advanced chemical vapor deposition graphene production technique and graphene transfer method are used to achieve the graphene interfaces. A number of nano-fabrication technologies are employed to fabricate various graphene interface samples with different contacting materials to conduct the research. The annealing effect will be studied through the thermal boundary resistance changes for different metal/graphene interfaces.
CHAPTER 2
THE 3ω MEASUREMENT TECHNIQUE

2.1 Fundamentals of the 3ω Method

The 3ω method, also known as the three omega method, was first introduced by Cahill in 1989 to measure the thermal conductivity of bulk dielectric materials[30], later it became a widely implemented method to measure the cross-plane thermal conductivities of thin films [31]. Further modification tuned it into a versatile method for measuring in-plane thermal conductivities of thin films and thermal boundary resistance [32, 33]. In general, the 3ω method is an electrical heating and sensing transient state measurement method.

2.1.1 Measurement principle

The 3ω method utilizes a patterned metallic strip as a heater to impose heat load into a sample and also a sensor to reflect the temperature variation on the surface of the sample.

As illustrated in Fig. 2.1, an AC current with angular modulation frequency ω and amplitude $I_0$ passes through a metallic strip, generating a heating source with power $P$

$$P = I_0^2 R_0 \sin^2(\omega t) = \frac{I_0^2 R_0}{2} - \frac{I_0^2 R_0}{2} \cos(2\omega t) \quad (2.1)$$

where $R_0$ represents the resistance of the metallic strip under experiment condition. Equation 2.1 describes that the heating source contains a fluctuation component oscillating at frequency $2\omega$. So the heating source generates a temperature fluctuation which also oscillates at frequency $2\omega$. 

![Fig. 2.1 Metallic strip and configuration (a) cross-section view and (b) top view.](image)
\[ T = T_0 + \Delta T_{2\omega} \cos(2\omega t + \varphi) \]  

(2.2)

where \( \varphi \) is the phase shift due to the thermal mass of the system. Since the resistance of the strip is a linear function against the temperature of the strip, a \( 2\omega \) fluctuation will be induced into the resistance variation,

\[ R = R_0 + \frac{dR}{dT} \Delta T_{2\omega} \cos(2\omega t + \varphi) \]  

(2.3)

where \( R_0 \) is the resistance of the strip at temperature \( T_0 \). Thus the voltage drop across the strip can be calculated by multiplying the current by the resistance,

\[
V = I_0 \sin(\omega t) \left[ R_0 + \frac{dR}{dT} \Delta T_{2\omega} \cos(2\omega t + \varphi) \right]
\]

(2.4)

\[
= V_0 \sin(\omega t) + \frac{V_0}{R_0} \left( \frac{dR}{dT} \right) \Delta T_{2\omega} \cos(2\omega t + \varphi) \sin(\omega t) 
\]

\[
= V_0 \sin(\omega t) + \frac{V_0}{R_0} \left( \frac{dR}{dT} \right) \Delta T_{2\omega} \frac{1}{2} [\sin(3\omega + \varphi) - \sin(\omega + \varphi)] 
\]

\[
= V_0 \sin(\omega t) - \frac{V_0}{R_0} \left( \frac{dR}{dT} \right) \Delta T_{2\omega} \frac{1}{2} \sin(\omega + \varphi) + \frac{V_0}{R_0} \left( \frac{dR}{dT} \right) \Delta T_{2\omega} \frac{1}{2} \sin(3\omega + \varphi) 
\]

\[
= V_{1\omega} \sin(\omega t + \gamma) + V_{3\omega} \sin(3\omega + \varphi)  
\]

(2.5)

From the derivation above, \( \Delta T_{2\omega} \) can be derived as

\[
\Delta T_{2\omega} = \frac{2V_{3\omega}}{aV_0}, \quad \alpha = \frac{1}{R_0} \left( \frac{dR}{dT} \right)
\]

(2.6)

where \( \alpha \) is the temperature coefficient of the resistance of the strip. Because of the small variation between \( V_0 \) and \( V_{1\omega} \), equation 2.6 can be approximated as

\[
\Delta T_{2\omega} \approx \frac{2V_{3\omega}}{aV_{1\omega}}  
\]

(2.7)

Following equation 2.7, the measurement utilizes a lock-in amplifier to detect the voltages with frequencies \( 1\omega \) and \( 3\omega \) by fixing \( V_{1\omega} \) as constant.
ΔT<sub>2ω</sub> represents the temperature rise of the metallic strip and is also regarded as the temperature rise of the sample surface. This approximation has been proven to be correct according to Kim’s investigation on the thermal boundary resistance of interface between metallic strip and target film, which shows that the temperature drop across such an interface is less than 1% of the total temperature drop. As shown in Fig. 2.2, ΔT<sub>2ω</sub> decreases as frequency increases. This relationship contains the thermal information of the sample, which will be discussed later.

### 2.1.2 Measurement apparatus and circuits

The measurement apparatus includes a probe station, a lock-in amplifier, and a signal process circuits. The lakeShore TTPX probe station is the main facility to conduct experiments. Fig. 2.3 gives an overall view of the full probe station system containing four major sub-systems. The vacuum cryostat, composed of a cryogen Dewar system, a turbo vacuum pumping system and a vacuum chamber with a refrigerator, can carry out experiments from 80K-350K under a maximum vacuum level of 10<sup>-6</sup> Torr. The precision temperature controller LakeShore 336, which can detect a temperature fluctuation of 0.001K, is used to monitor the temperatures of the components of the system and heat the system actively to ensure that experiments are conducted under a very small temperature fluctuation, typically less than 0.05K. Meanwhile, maintaining a high vacuum condition during experiments is necessary to eliminate heat convection between samples and environment atmosphere. The integrated probes station and 18pins socket are used to input and detect
electrical signals according to experiments schemes. Combined with an optical microscope, the system can carry out flexible operation for different experiments through manipulation of the probes and connection.

A Lock-in amplifier is used to detect and measure very small AC signals - all the way down to a few nanovolts. Accurate measurements can be taken even when a small signal is obscured by noise sources of magnitude many thousands of times larger. A Lock-in amplifier uses a technique known as the phase-sensitive detection to single out the components of the signal at specific reference frequencies and phases. Noise signals at frequencies other than the reference frequency are rejected and do not affect the measurement. Thus, the Lock-in amplifier allows the isolation of signals at $1\omega$ and $3\omega$, which is the foundation for successful experiments. The Stanford Research System SR830 Lock-in amplifier is used here [4].
The lab-made signal processing circuit board is used to collect signals from the samples and preliminarily process the signals for a later Lock-in amplifier function. The two AD524CD amplifiers serve as differential devices rather than voltage amplifiers to obtain the voltage difference between the two electrode pads of the patterned metallic strip and subtract the common background noise from the environment. The AD7541A KN, AD744KN, 33Ω resistor, 100Ω resistor and 33pF capacitor comprise a negative multiplication circuit to calibrate the resistance of the metallic strip in experiment. The two high precision potentiometers with an ultralow TCR are used to balance the resistance of the strip, which functions as a preliminary noisy reductor. The calibration and balance process is as follows: an AC source with an amplitude of 0.5V at 33Hz is first applied to the sample-potentiometer serial circuit and the potentiometer is set to a value larger than the resistance of the metallic strip. By the manipulation of the input modes of SR830, it can detect 1ω voltage signals for both the strip and potentiometer; after that the voltage ratio between strip and potentiometer is calculated by a computer and later converted to binary codes for the multiplication circuit. Thus, the large 1ω noise can be reduced in the next 3ω detection through this voltage balancing.

Fig. 2.5 Circuit digram.
The SR830 Lock-in amplifier and circuit board is controlled by a LabVIEW program during experiment. Data are recorded automatically by a computer for further analysis. Following the calibration and balancing process, the SR830 Lock-in amplifier generates a sine source with a larger amplitude which is applied to the strip-potentiometer circuit. Using the four wires measurement, the $1\omega$ voltage signal coming from the metallic strip is detected by the SR830 lock-in amplifier and treated as a constant during the measurement. Through manipulation of the SR830 Lock-in amplifier, the $X$ value of the $3\omega$ voltage signals of different frequencies is detected in the differential input mode for noise elimination purpose.

![Schematic of the measurement system](image1)

Fig. 2.6 Schematic of the measurement system.

![Photo of the Lakeshore probe station](image2)

Fig. 2.7 Photo of the Lakeshore probe station.
2.1.3 Data reduction

The general model for a two dimensional \( n \) layers anisotropic films on a substrate model is expressed as [33]

\[
\Delta T = \frac{-P}{\pi l k_{y1}} \int_{0}^{\infty} \frac{1}{A_{i}B_{1}} \frac{\sin^2(b\lambda)}{b^2\lambda^2} d\lambda
\]

(2.8)

where

\[
A_{i-1} = \frac{A_{i} \frac{k_{yi}B_{i}}{k_{yi-1}B_{i-1}} - \tanh(\varphi_{i-1})}{1 - A_{i} \frac{k_{yi}B_{i}}{k_{yi-1}B_{i-1}} \tanh(\varphi_{i-1})}, \quad i = 2, 3, \ldots n,
\]

\[
B_{i} = \sqrt{(k\lambda^2 + \frac{i2\omega}{\alpha_{yi}})}, \quad i = 1, 2, \ldots n,
\]

\[
\varphi_{i} = B_{i}d_{i}, \quad k_{xyi} = \frac{k_{xi}}{k_{yi}}
\]

In the above expressions, \( n \) is the total number of layers including the substrate, subscript \( i \) corresponds to the \( i \)th layer starting from the top, subscript \( y \) corresponds to the cross-plane direction, \( b \) is the half width of the metallic strip, \( k \) is the thermal conductivity of each layer, \( \omega \) is the angular modulation frequency of the electrical current, \( d \) is the layer thickness, and \( \alpha \) is the thermal diffusivity. The effect of thermal conductivity anisotropy is introduced through the term \( k_{xy} \), which is the ratio of the in-plane to cross-plane thermal conductivity of the layer.

For the substrate layer \( i=n \), and if the substrate is semi-infinite \( A_{n} = -1 \). When the substrate has a finite thickness, the value of \( A_{n} \) depends on the boundary condition at the bottom surface of the substrate: \( A_{n} = 2\tanh(B_{n}d_{n}) \) for an adiabatic boundary condition or \( A_{n} = -1/\tanh(B_{n}d_{n}) \), if the isothermal boundary condition is considered. By fitting the parameters of the model, thermal conductivities in cross-plane direction and in-plane direction of each layer can be obtained. A Matlab code to fit the general mode is developed and shown in Appendix. But for substrate only and one layer film on the substrate samples, there are other approaches to analyze the data to simplify the procedure.

The simplest data reduction model was proposed by Cahill in 1990 [30] to obtain the thermal conductivity of isotropic bulk solids, or referred to as substrates. This model assumes
the metallic strip as a line heating source and the substrates as a semi-infinite solid. The thermal model can be approximated by Eq. 2.7, which describes the relationship between the temperature rise $\Delta T$ of the metallic strip and the frequency of the sine source.

\[
\Delta T = \frac{P}{\pi l k_s} \left( \frac{1}{2} \ln \frac{\alpha_s}{b^2} + \delta \frac{1}{2} \ln (2\omega) - \frac{\nu}{4} \right) \tag{2.9}
\]

In this equation, $P$ is the power applied in the metallic strip, $l$ is the length of the metallic strip, $\alpha_s$ is the thermal diffusivity of the substrate, $b$ is the half width of the metallic strip, $\delta$ is a constant approximated to be 0.923, $\omega$ is the angular frequency of the source, and $k_s$ is thermal conductivity of the substrate. Eq. 2.7 indicates that the $\Delta T$ contains a real part and an imaginary part and both of them can be used to derive the thermal conductivity $k_s$. Cahill suggests that using the real part gives a better accuracy in the derivation. So that is why in the $3\omega$ voltage detection process the X value which stands for the real part is recorded rather than the R value. Taking the derivation of this equation, with respect to $\ln(2\omega)$, the relationship can be expressed as

\[
\frac{P}{2\pi l k_s} = \frac{d(\Delta T)}{d(\ln 2\omega)} \tag{2.10}
\]

so the left side of Eq. 2.10 is the slope of the linear relationship between $\Delta T$ and $\ln(2\omega)$ and $k_s$ can be calculated by Eq. 2.10. This method is called the slope method.

Later, Cahill developed the slope method for the thermal conductivity of dielectric thin films. In this measurement scheme, the heat transport inside the thin film is considered as one dimensional heat conduction in the cross-plane direction of the thin film. This assumption means the thin film does not change the heating profile inside the substrate, in other words, the thin film is like an additional thermal resistance underneath the metallic strip and has the same shape.

![Fig. 2.8 Illustration of the slope method for a thin film sample.](image-url)
Thus, according to the Fourier equation the temperature difference across the thin film $\Delta T_F$ can be expressed as

$$\Delta T_F = \frac{P t_F}{2b l k_F}$$  \hspace{1cm} (2.11) \nonumber

where subscript F denotes the thin film, $t_F$ is the thickness, and $k_F$ stands for the thermal conductivity of the thin film. In this model, the temperature rise of the metallic strip is the sum of the temperature rise of the substrate $\Delta T_S$ and $\Delta T_F$.

$$\Delta T_{S+F} = \Delta T_S + \frac{P t_F}{2b l k_F}$$  \hspace{1cm} (2.12) \nonumber

$\Delta T_S$ can be calculated by Eq. 2.7 with the imaginary part disregarded and $k_S$ is obtained by the slope method. By the subtraction of $\Delta T_S$ from $\Delta T_{S+F}$, $k_F$ is derived.

![Data plot of 1μm SiO2 thin film on Si wafer by the slope method.](image)

Fig. 2.9 Data plot of 1μm SiO2 thin film on Si wafer by the slope method.

To achieve a high accuracy with the slope method, the semi-infinite substrate and line heating source model, and the one dimensional heat conduction in thin film assumption must be valid. T.Borca made a comparison between the approximated slope from the slope method and the analytical slope generated from the general model and proposed the quantificational criteria for evaluation of the measurement for isotropic substrate in 2001 [33]. The thermal penetration depth $L_{\alpha}$ is taken into consideration.

$$L_{\alpha} = \frac{\alpha_S}{\sqrt{2\omega}}$$  \hspace{1cm} (2.13) \nonumber
$L_\alpha$ physically represents the distance a thermal wave travels at a certain frequency $\omega$. When $L_\alpha$ is five times larger than the half width $b$ of the metallic strip, the line heating source assumption is valid; however when $L_\alpha$ is less than one fifth of the thickness of substrate $d_s$, the semi-infinite model is acceptable. In summary, when the thickness of the substrate is at least 25 times larger than the half width of the metallic strip, a suitable frequency range will exist to achieve inequality below which the approximation of the slope method gives at least a 99% accuracy.

$$5b < L_\alpha < \frac{d_s}{5}$$  \hspace{1cm} (2.14)

For a typical Si wafer structure with a thickness of 400 $\mu$m and a widely used 30 $\mu$m wide metallic strip, $L_\alpha$ must be larger than 75 $\mu$m but smaller than 80 $\mu$m. The thermal diffusivity of silicon is $8 \times 10^{-5}$ m$^2$/s, by applying $L_\alpha$ equation, the best range of frequency that would result in a 99% accuracy of thermal conductivity for substrate is from 700 Hz to 1300 Hz.

For the one dimensional heat conduction in thin film assumption, the criteria are more complex. To keep the assumption to be valid, the heat spreading effect inside a film should be minimized. A parameter $\beta_F$ is used to describe the effect caused by the anisotropy of thermal conductivities in different directions of a film and the ratio between the film thickness and the half width of the metallic strip.

$$\beta_F = \frac{t_F}{b} \sqrt{k_{xy}}$$  \hspace{1cm} (2.15)

where $k_{xy}$ is the anisotropy, the ratio between the in-plane thermal conductivity and the cross-plane thermal conductivity of a film. When $\beta_F$ is smaller than 0.1, the assumption is valid for the slope method since the assumption will only introduce an error of less than 3%. If $\beta_F<0.1$ is not realized, but $\beta_F<10$, the heat conduction can still be considered as one dimensional if the width of the heater is replaced by a corrected width used for calculation as

$$b' = 2b + 0.76t_F \sqrt{k_{F,xy}}$$  \hspace{1cm} (2.16)

which generates an error of within 3%, the same as the $\beta_F<0.1$ case.
Fig. 2.10 Accuracy of results depending on the $\beta_F$ and $kr_{F/S}$. $K_{Fy}/K_{1D}$ is the thermal conductivity ratio between that deduced from the general model and that from 1D heat conduction assumption, the higher the ratio, the better the accuracy [33].

Another factor that adversely affects the measurement is the contrast of the film/substrate thermal conductivities. This is easily understood because in the limiting case of a semi-infinite substrate and $k_S$ equal $k_F$, the temperature drop across film $\Delta T_F$ would be zero, if we disregarded the thermal boundary resistance between the film and substrate. Also if the thermal conductivity of the thin film was much larger than the thermal conductivity of substrate, the temperature drop of thin film would become very small. This requires a very high sensitivity in the measurement system making the accuracy of the result questionable. So the 3ω method is the most suitable for the case with a low ratio of film/substrate thermal conductivity. The ratio $kr_{F/S}$ is introduced to evaluate the effects. If $kr_{F/S}$ is smaller than 0.1, the film/substrate contrast effect is negligible.

$$kr_{F/S} = \frac{\sqrt{k_{Fy}k_{Fx}}}{k_S}$$  \hspace{1cm} (2.17)

If the sample structure becomes more complex, there is still another method called the differential method to avoid the fitting of the general model. In this method, a reference sample with the same structure, same material, same dimension and same processing procedure, but without the target thin film, is used for comparison and subtraction.
In this method, the absence of the target film in the reference sample is considered to play no effects on the other parts of the sample. This method provides an easy way to extract the thermal conductivity of the target thin film from a multi-layer structure. But to maintain a high accuracy in measurement, the reference sample must be as similar as possible to the target sample, this is because the differential method is very sensitive to variations between samples.

In order to maintain the same accuracy, the validity of the assumptions for the slope method also is the criteria to evaluate the differential method. For the differential method, the principal equation is transformed to

\[ \Delta T_{\text{sample}} = \Delta T_{\text{reference}} + \frac{P t_F}{2b l k_F} \]  

(2.18)

By measuring the temperature rises of the target sample and reference sample under the same heat load, the thermal conductivity of the target thin film is easy to obtain. Also, if the heat load in two samples are not easy to control to be the same, calculating the temperature rise per unit power for each sample is an alternative way to deduce the thermal conductivity of the target thin film.

The slope method and differential method are the most widely used approach to analyze the data obtained by the 3ω method. Through the careful design of the sample structure such as the geometry of the metallic strip and the substrate thickness under the criteria, the challenge faced in determining cross-plane thermal conductivity can be met. For some specific purposes, the modified methods will be discussed later.
2.1.4 The 3ω method for thermal boundary resistance

The differential method can be extended to measure the thermal boundary resistance for an interface. The requirement for this extension is that there is one film of high cross-plane thermal conductivity and small thickness [34]. The model of the differential method is recalled, and the principle equation is modified as

\[ \Delta T_{\text{sample}} = \Delta T_{\text{reference}} + \frac{Pr_F}{2bk_F} + \frac{P}{2bl}(R_{th}^{\text{upper}} + R_{th}^{\text{lower}}) \]  \hspace{1cm} (2.19)

where \( R_{th}^{\text{upper}} \) is the thermal boundary resistance between the top layer and the target film and \( R_{th}^{\text{lower}} \) is the thermal boundary resistance between the target film and the bottom layer. Therefore the last term in the equation represents the sum of the temperature drop across the two interfaces by using the Fourier equation. As mentioned, \( t_F \) is very small and \( k_F \) is very big, so the second term in the equation, representing the temperature drop across the target film, is very small and can be neglected. For example, a 100nm aluminum thin film with a thermal conductivity of 250 W/(m*K) has an equivalent thermal resistance only of \( 4*10^{-10} \) m²*K/W, which is at least one order of magnitude lower when compared with a typical thermal boundary resistance which is always larger than \( 10^{-9} \) m²*K/W. Thus, the principle equation can be simplified as

\[ \Delta T_{\text{sample}} = \Delta T_{\text{reference}} + \frac{P}{2bl}(R_{th}^{\text{upper}} + R_{th}^{\text{lower}}) \]  \hspace{1cm} (2.20)

which means that the target film is treated as the thermal boundary resistance of two interfaces connected in series. If the top layer and the bottom layer are of the same material, \( R_{th}^{\text{upper}} \) is equal to \( R_{th}^{\text{lower}} \). By applying the differential method and solving equation 2.9, the thermal boundary resistance of the interface between the target film and the contacting material can be obtained. It should be noted that the basic assumptions for applying the differential method still need to be validated.
2.1.5 The 3ω method for anisotropy measurement

If the anisotropy of the substrate or the thin film has to be measured, an additional narrow metallic strip is required. The reason for this scheme is that the narrow metallic heater can generate efficient amount of heat spreading effect, making the temperature rise sensitive to the in-plane heat conduction contribution.[35, 36]

After the temperature rise of two different metallic strips is obtained, and the cross-plane thermal conductivity is solved by the slope method or the differential method, the in-plane thermal conductivity of the target thin film can be set as the free parameter in the general model. By adjusting the parameters, the temperature rise obtained from the general model is fitted to the one obtained experimentally from the narrow metallic strip. As the thermal conductivities of two directions are obtained, the anisotropy of thermal conductivity is available.

2.2 Advantages and limitations of the 3ω method

The 3ω method is a robust measurement method for films-on-substrate samples. It utilizes the Lock-in amplifier to detect the small 3ω signal, so it is sensitive to a very small temperature rise, which is the most difficult problem for conventional thermal conductivity
measurement techniques. It has been applied to measure thermal conductivities of thin films with thicknesses ranging from 20nm to 5μm. By using the quantificational guidelines to design the width of the metallic strip, a high accuracy can be achieved following the specific requirements. Because of the small power AC source used in experiments, the heat will only affect a small region near the strip heater. That means the size of the samples normally is small, but just large enough to fit the assumption. Another advantage is that it is a non-destructive method. Samples will not be damaged during the measurement so the results are regarded as the intrinsic value. Last but not the least, the arrangement of instruments, component integration, and equipment operation are easy to implement. The initial cost of the system is low when compared with other thermal conductivity measurement systems for thin films [37].

As the 3ω method utilizes electrical heating, thus, electrical isolation between the metallic strip and the target sample is necessary. For electrically conductive samples, an additional dielectric thin film must be deposited on the surface of the samples to avoid electrical leakage which destroys the measurement. Due to the small scale of the strip, typically in the micrometer range, micro-fabrication technology and pattern processes are always involved. Care should be exercised during these fabrication steps to eliminate any uncertainty from sample preparation. Since the metallic strip only heats up the nearby region, the measured results are the local thermal conductivities for those regions. In other words, if a sample is not uniform and variation exist in different regions, the 3ω method may not give stable results, making it hard to determine the overall thermal conductivity of such a sample. When there are several target films to measure, multiple samples must be fabricated to extract the thermal conductivity for each film if the differential method is applied.

2.3 Verification of the 3ω method system

To verify the measurement system, the well characterized amorphous SiO₂ film and Si wafer are used for both the slope method and the differential method. The samples used for verification are 400μm bare Si wafer and 400μm Si wafer with a 1μm thick SiO₂ on top. The patterned metallic strip consists of 100nm Pt with a 10nm Cr adhesion layer and the dimensions are 30μm wide and 1mm long with four electrode pads for electrical connection. To pattern the metallic strip, photo-lithography is used and E-beam physical vapor deposition (PVD) is employed to deposit the metals.
To verify measurement, validation of the $3\omega$ method assumption is carried out first. For the semi-infinite model, the ratio of the substrate thickness to the half width of the strip is $400/15=26.4$, which is larger than 25; for the one-dimensional heat conduction assumption, the anisotropy $k_{xy}$ of amorphous SiO$_2$ film is treated as 1 and so $\beta_F$ is $1/15*1=0.067$, which is less than 0.1. Therefore, the geometries of samples and metallic strip are suitable for the $3\omega$ method. The verification experiment is conducted at room temperature at around 300 K and under a vacuum condition of $10^{-5}$ Torr. The experiments were carried out separately on Si wafer and SiO$_2$/Si wafer. The data are processed and plotted in Fig. 2.15

After the data are processed, the thermal conductivities of Si wafer and amorphous SiO$_2$ film are obtained and shown in table 2.1. Both the slope method and the differential method show the similar result for amorphous SiO$_2$ film, around 1.3 W/m·K. These results are consistent with the reported value from literature and materials properties database which are ranges from 1.2 to 1.5 W/m·K. For Si thermal conductivity, compared with the typical value for Si, which is around 140 W/m·K, both samples give a 10% different when compared to the typical value. The Si thermal conductivity from the SiO$_2$/Si sample is lower than the one
obtained from the bare Si sample, this is because the SiO$_2$ film serves as additional thermal resistance to Si, decreasing the effective thermal conductivity of the whole sample when compared with that of the bare Si sample. Recalling the film/substrate contrast factor, the results need to be tested for this factor to ensure its reliability. The amorphous SiO$_2$ film is treated as isotropic, and $k_{f/S}$ is 1.3/129=0.01, which is less than 0.1. So the result excludes the error from the film/substrate contrast effect.

Table 2.1 Thermal conductivity obtained from verification experiment, W/m·K.

<table>
<thead>
<tr>
<th></th>
<th>SiO$_2$</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slope method</td>
<td>1.30</td>
<td>129 for SiO$_2$/Si</td>
</tr>
<tr>
<td>Differential method</td>
<td>1.31</td>
<td>154 for bare Si</td>
</tr>
</tbody>
</table>

Thus, our 3ω method system has been successfully set up and its accuracy is demonstrated by the verification measurement on amorphous SiO$_2$ film samples for both the slope method and the differential method.
CHAPTER 3
THERMAL BOUNDARY RESISTANCE BETWEEN GRAPHENE AND AMORPHOUS ALUMINUM OXIDE AND BETWEEN GRAPHENE AND ALUMINUM

3.1 Background

Graphene is the first material with a 2D structure existing in nature. Its discovery by A. K. Geim and K. S. Novoselov in 2004, was followed by ten years of intense researches to understand the unique properties and promote application [11].

![Graphene Schematic](image)

Fig. 3.1 Graphene is a 2D building material for carbon materials for all other dimensionalities [11].

Owing to its one-atom-thick hexagonal fabric of carbon atoms structure, graphene exhibits many unusual properties. The electron mobility of graphene is above 10,000 cm²/V·s which is one order of magnitude higher than the charger carrier mobility of doped silicon. This extraordinary property has highly attracted researchers to fabricate fast graphene transistors, especially field effect transistor (FET) [26]. A graphene FET consists of source, drain, gate, gate dielectric and the graphene conduction channel which is a kind of semiconductor in conventional FETs. To achieve high performance and maintain a small size at the same time, a high dielectric constant material is required. In recent years, researchers have successfully integrated graphene and aluminum oxide whose dielectric constant is 3
times that of silicon oxide. By applying a Al seed layer to initiate the deposition of aluminum oxide, Kim realized a graphene FET combined with an atomic layer deposition (ALD) aluminum oxide [24]. The device showed mobility values of over 8000 cm²/V·s at room temperature. Lei et al demonstrated a graphene FET by directly transferring Al₂O₃ nanoribbons on top of a graphene sheet. This approach preserved the pristine nature of graphene and allowed the device to reach its highest mobility up to 23600 cm²/V·s [25]. As graphene is very flexible, Lu et al used PET as the substrate to assemble a flexible graphene FET. They oxidized a thin layer of Al to form AlOₓ as the gate dielectric [38]. These experiments prove the feasibility of graphene FETs and the promising performance means breakthroughs in microelectronics would be forthcoming if a graphene generation arrives. But most of these graphene FETs used the mechanically exfoliated graphene sheets from highly oriented pyrolytic graphite (HOPG) as the graphene source which is only for the purpose on concept demonstration in lab. Another point to consider is that the large variation of mobility obtained by different devices. If the graphene/dielectric interfaces in graphene FETs were of a high quality and the devices kept the pristine nature graphene [25], the devices would be believed to be high performance ones.

Aside from using mobility as a measure of the performance of graphene FETs, a critical issue that remains is the heat generation and dissipation in graphene FETs. When a large current is passed through graphene FETs or a high switch frequency is applied on the FETs, the heat generated by electrical power will raise the operating temperature of FETs. As a
result, the properties of graphene are degraded and thermal management may fail. The major paths to dissipate heat inside the FETs are through the active zone of graphene which is in contact with the bottom insulator and the top gate dielectric [27]. Because the graphene layer is only one-atom thick and the thickness of the dielectric and bottom insulator should be small, the thermal boundary resistance of the graphene interfaces becomes the most important parameter to specify the thermal management issue. A previous study to determine the thermal boundary resistance of the interface between graphene and silicon oxide was carried out by Chen et al. They fabricated 3D devices on top of the sandwich structure with the graphene imbedded in the two layers of silicon oxide. The thermal boundary resistance values at room temperature ranged from $5.6 \times 10^{-9}$ to $1.2 \times 10^{-8} \text{ m}^2 \text{K/W}$ [16]. Such small values proved the potential of graphene application in microelectronics. However, the graphene in that measurement was also obtained by mechanical exfoliation which only guaranteed the performance of graphene FETs fabricated by the lab processes rather than the industry compatible processes.

High-quality large scale graphene production is one of the prerequisites for bring about the graphene generation and the first step to realize industry compatible graphene microelectronics. The most promising method is chemical vapor deposition (CVD) [23]. Applying this method, graphene is produced on copper foils and a transfer step is necessary to convey the graphene to target substrates. Although the transfer is as complicated as the production and there may be a large amount of residue left on the surface of graphene, CVD graphene is still considered the most plausible way to effectively produce graphene in a relatively low price. The residue can be eliminated by post processes [28].

Fig. 3.4 Quality vs. price of different method [23].
From the above discussions, to pave the road for mass production graphene FETs, there are two issues that need pre-examining. First, the interface quality between graphene and contacting materials has a big influence on graphene performance. But the difference in interface quality between mechanical exfoliated graphene and CVD graphene is not clear. Second, heat dissipation in graphene FETs must be evaluated for CVD graphene FETs with new contacting materials. With the combination of these two issues and the consideration of thermal aspects, the focus of this study is the characterization on the thermal boundary resistance of the interface between CVD graphene and aluminum oxide.

3.2 Materials and fabrication procedure

To fabricate suitable samples to carry out the measurement, some common nanofabrication technologies are applied and advanced CVD graphene production and transfer are introduced. A brief description of the procedures is shown below.

3.2.1 CVD graphene growth on copper foil

Graphene grown by CVD on Cu foil is the most promising technique to scale up graphene production. The Cu foil serves as a catalyst to promote graphene deposition. CH₄ is the precursor in this growth method. Through controlling the amount of precursor gas, it is easy to control the number of layers of graphene under an optimal growth condition. In this study, to reduce the contribution of graphene in heat conduction, single-layer graphene is used so that the thermal resistance from graphene can be neglected. All the graphene used in this study is single-layer but polycrystalline.

![Deposition and mechanism of CVD graphene grown on Cu.](image)

Fig. 3.5 Deposition and mechanism of CVD graphene grown on Cu.
3.2.2 Graphene transfer

In our experiments, graphene is transferred by using Poly (methyl methacrylate) (PMMA) as media. The graphene transfer includes PMMA coating, Cu foil etching, and PMMA removing.

Fig. 3.6 Schematic illustration of the processes to transfer graphene by PMMA.

3.2.3 Atomic layer deposition (ALD) Al₂O₃

ALD aluminum oxide deposition is a very precise deposition technology. Through controlling the deposition cycles, the thickness of the Al₂O₃ can be increased by one atom layer per cycle. The advantage of utilizing ALD Al₂O₃ in thermal boundary resistance measurement is that depending on the accurate control of thickness, the variation of thermal resistance induced by amorphous ALD Al₂O₃ which is a poor thermal conductor can be eliminated. Thus the accuracy in thermal boundary determination is improved.

3.2.4 Electron beam physical vapor deposition (EBPVD) of metal

Electron Beam Physical Vapor Deposition (EBPVD) is a form of physical vapor deposition in which a target anode is bombarded with an electron beam given off by a charged tungsten filament under a high vacuum. The electron beam causes atoms of the target to transform into the gaseous phase. These atoms then precipitate into a solid form, coating everything in the vacuum chamber (within line of sight) with a thin layer of the anode material. EBPVD-metal provides good control of the deposition rates and surface flatness. Under a same recipe, this kind of deposition will give the best consistency in metal quality which is very important for our experiments.
3.2.5 Shadow mask patterning

Shadow mask patterning is a common tool to define metal patterns on a target substrate. Usually, a shadow mask is made from a metal or graphite sheet by cutting away the desired patterns. The feature size of the pattern on a shadow mask can reach 5 µm. As illustrated in Fig. 3.5, the shadow mask is placed on top of the target substrate. During the deposition process, the metal will cover the entire surface including the shadow mask, but for the substrate, only the surface exposed by the patterned holes can receive the deposited metal atoms. The shadow mask is fixed on top of the substrate by tapes so the assembly and detachment is very simple. Thus shadow mask patterning is a very efficient and convenient method to fabricate patterns at micrometer level.

![Fig. 3.7 Principle of shadow mask patterning, the upper plate is a shadow mask.](image)

3.2.6 Inductive coupled plasma (ICP) etching

ICP etching is a kind of reactive ion etching. The plasma etchant, typically plasma from oxygen or fluorine-bearing gas, is generated with an RF powered magnetic field. A separate RF bias is applied to the substrate to create directional electric fields near the substrate to achieve more anisotropic etch profiles. Through this method, a vertical etching against the substrate surface is achieved.

![Fig. 3.8 Typical ICP etching setup.](image)
3.2.7 Sample fabrication and devices integration

A commercial Si wafer is used as the substrate for subsequent fabrication processes. A 50 nm layer of ALD Al₂O₃ is first deposited on the surface of the Si wafer. Then a graphene sheet is transferred to cover the surface of Al₂O₃, and this is followed by an annealing process to further remove the polymer residue. After that, a 2 nm Al seed layer is deposited by EBPVD and oxidized naturally in order to trigger a second deposition of 50 nm ALD Al₂O₃ as uniformly as possible. This step is resulted from the chemical inertness of the graphene surface. The ALD Al₂O₃ process must first react with target surface to form nucleation sites, while only the defects or grain boundary in the graphene sheet can provide the dangling bonds to initiate deposition. So, the direct deposition of uniform ALD Al₂O₃ is hardly realized and an Al seed layer is the most acceptable way to maintain the quality of later ALD Al₂O₃ [24].

Fig. 3.9 Flow chart of the fabrication process.

Next, the $3\omega$ devices will be deposited on top of the structure by a combination of shadow mask and EBPVD metals. The shadow masks used in this fabrication are stainless steel sheet with a total of 40 patterns. The shape of the patterns is a typical four wire measurement $3\omega$ devices with a geometry similar to that shown in chapter 2. The width of the metallic strips which is the most critical dimension in the $3\omega$ method is 30 μm. An adhesive Cr layer of 10 nm thick is deposited before deposition of a 200 nm Pt layer. Due to the chemical inertness and large TCR of Pt, it is the best material for the electrodes. Actually, during the metal deposition, part of metal may stick to the sidewalls of the shadow masks. As a result, the devices cannot form the exact same shape of the pattern, and the actual width of the metallic strips is measured to be around 20 μm. Finally, the whole sample is put in a ICP
etching machine to remove the part that is not covered by the metal. The reason for implementing this step is to eliminate the spread of heat inside the graphene sheet due to the ultrahigh in-plane thermal conductivity of graphene. Therefore, the one dimensional heat conduction model in the $3\omega$ method is maintained.

As the final sample structure in Fig. 3.7 shows, the structure underneath the $3\omega$ device has a graphene sheet sandwiched by two layers of ALD Al$_2$O$_3$. For the interface between the graphene and the Al seed layer, we assume the natural oxidation process will completely convert the Al to Al$_2$O$_3$, yielding another graphene/Al$_2$O$_3$ interface which is regarded as the same as the bottom Al$_2$O$_3$/graphene interface. So there two graphene/Al$_2$O$_3$ interfaces connecting serially by graphene. Due to the fact that graphene sheets are only one atomic thick, the thermal resistance of graphene itself is neglected. Thus, the insertion of graphene only creates two interfaces. Recalling the principle equation of the $3\omega$ method for interface,

$$\Delta T_{\text{sample}} = \Delta T_{\text{reference}} + \frac{P}{2bl} (R_{th}^{\text{upper}} + R_{th}^{\text{lower}})$$

(3.1)

To extract the thermal boundary resistance, a reference sample without graphene is required. The reference sample is fabricated along with the processes of the graphene sample. The total thickness of the two layers of Al$_2$O$_3$ is 100 nm, same as the graphene sample, and the Al$_2$O$_3$/Al$_2$O$_3$ interface caused by the two separated deposition processes is ignored because of the consistency of the material.

![Fig. 3.10 Explanation of the extraction of thermal boundary resistance.](image)

Thus, the final equation to calculate thermal boundary resistance is

$$R_{th} = \frac{bl \times (\Delta T_{\text{sample}} - \Delta T_{\text{reference}})}{P}$$

(3.2)

Applying the same scheme, another four kinds of samples are fabricated for more information on thermal boundary resistance. All the samples start with the deposition of a Al$_2$O$_3$ layer serving as the barrier layer to prevent the diffusion of metal atoms into the silicon.
substrate and end up with the deposition of a second Al₂O₃ layer serving as the insulating layer to isolate the electrical current from the metal and graphene.

![diagram](image)

**Fig. 3.11 Three different kinds of structure for thermal boundary resistance measurement:** (a) Al/graphene/Al; (b) Al₂O₃/graphene/Al; (c) Al/graphene/Al₂O₃; (d) Al₂O₃/Al/Al₂O₃.

The Al/graphene/Al sample is used to characterize the thermal boundary resistance between graphene and Al. The fabrication procedure is almost the same as the Al₂O₃/graphene/Al₂O₃ sample, while there are two layers of Al deposited separately before and after graphene transfer. The Al is deposited by the EBPVD method and the thickness of each Al layer is 50 nm. Furthermore, using the similar processes, the Al₂O₃/graphene/Al and Al/graphene/Al₂O₃ are made and used to investigate the heterogeneous effect on the thermal boundary resistance of graphene interfaces. For these three kinds of structure, it is necessary to fabricate the reference samples with an Al layer of the same thickness, through which the thermal boundary resistance of Al₂O₃/Al is obtained by using the pure Al₂O₃ sample as the reference sample.

### 3.3 Thermal boundary resistance characterization

The thermal boundary resistance is characterized by the 3ω method which has been demonstrated before. The measurement is carried out in room temperature and the chamber of the probe station LakeShore TTPX was pumped to a vacuum state of 10⁻⁵ torr. The vacuum condition eliminated the heat loss from the heat convection between samples and the gas environment.

<table>
<thead>
<tr>
<th>Si wafer thickness</th>
<th>Metallic strip half width</th>
<th>Multilayer structure thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 μm</td>
<td>10 μm</td>
<td>100–200 nm</td>
</tr>
</tbody>
</table>

Table 3.1 Summary of the geometries of the sample structures.
Before the measurement, the assumptions made to ensure the validity of $3\omega$ method must be examined. For the semi-infinite substrate assumption, the thickness of the substrate should be more than 25 times the half width of the metallic strip to make sure that there exist an optimal frequency regime. In our design, the thickness of the Si wafer is 400 $\mu$m and the half width of the metallic strip is 10 $\mu$m, the ratio is 40, which is larger than 25. Thus the optimal frequency regime for our samples is within the range of 700 Hz to 2000 Hz. As the samples structure has been intentionally etched to attain a wall-like geometry to eliminate the heat spreading effect, the one dimensional heat conduction assumption is always valid in our experiments.

### 3.3.1 Thermal boundary resistance of the graphene/Al$_2$O$_3$ interface

For the Al$_2$O$_3$/graphene/Al$_2$O$_3$ sample, among the 40 devices, six devices survived the whole process. $3\omega$ measurement was performed on each workable device under the same condition. The reference sample was the 100 nm Al$_2$O$_3$ film. By comparing it to the same reference device measured under the same condition, the thermal boundary resistance of the six devices can be obtained.

![Fig. 3.12 Plot of a device data with linear regression.](image)

Fig. 3.12 shows a characterization plot of a pair of measurements, including the graphene sample and the reference sample. The linear coefficient indicates the quality of the data set. Both the graphene sample and the reference present a linear coefficient above 0.99, which means the data set is highly reliable. During measurement, if the electrical leakage occurred from the metallic strip to the conductive layer in the structure, or the structure was damaged, the linearity of the obtained data would be destroyed. Another parameter needing attention is the slope of the fitting line. In the $3\omega$ method, the slope can be used to calculate the thermal...
conductivity of the substrate, which is also used to evaluate the reliability of the measurement. The thermal conductivity of the substrate of the graphene sample is determined to be 126 W/m·K and for the reference sample the thermal conductivity of substrate is 149 W/m·K. Both results are close to the standard thermal conductivity of Si wafer which is around 140 W/m·K. The closely matching of the thermal conductivities of substrates of two samples increases the accuracy of the differential method. Thus, based on this pair of data and Eq. 3.1, we calculate the thermal boundary resistance of graphene/Al\textsubscript{2}O\textsubscript{3} interface in the sample shown in Fig. 3.12 to be 8.3*10^{-8} K·m\textsuperscript{2}/W.

![Graph](image)

Fig. 3.13 Summary of the results of six devices.

Fig. 3.11 summarizes the thermal boundary resistance of 6 devices. According to the results, a large variation is apparent for the one order difference between the highest result and the lowest result. All the results fall into the range of 10^{-8}~10^{-7} K·m\textsuperscript{2}/W.

### 3.3.2 The thermal boundary resistance of graphene/Al interface

To obtain the thermal boundary resistance of the graphene/Al interface, the sample consisting the Al\textsubscript{2}O\textsubscript{3}/Al/graphene/Al/Al\textsubscript{2}O\textsubscript{3} structure is used and the reference sample is Al\textsubscript{2}O\textsubscript{3}/Al/Al\textsubscript{2}O\textsubscript{3} in which the thickness of Al is 100 nm, which the sum of two layers of Al in the graphene sample. Fig. 3.14 shows a data plot of the Al\textsubscript{2}O\textsubscript{3}/Al/graphene/Al/Al\textsubscript{2}O\textsubscript{3} sample and the appearance is quite similar to the Al\textsubscript{2}O\textsubscript{3}/graphene/Al\textsubscript{2}O\textsubscript{3} sample in the previous section.
From the fitting results in the figure, the quality of the measurement is shown to be good because the linear coefficients of both data sets are approaching 1. The thermal conductivities of this pair of samples are determined to be 118 W/m·K for the graphene sample and 123 W/m·K for the reference sample. Thus, accuracy is maintained for this measurement. Thus, the thermal boundary resistance of the graphene/Al interface of the sample shown in Fig. 3.14 is calculated to be $9.2 \times 10^{-8}$ K·m²/W.

Fig. 3.15 Summary of the results of eight devices.

Fig. 3.13 summarizes the thermal boundary resistance of the eight working devices in the Al/graphene/Al sample. From the figure, a much narrower distribution of the results is shown when compared to the Al₂O₃/graphene/Al₂O₃ sample. The maximum thermal boundary
resistance is about twice the lowest one. All the results are also in the range of \(10^{-7}~10^{-8}\) K·m\(^2\)/W, but in a more concentrated range.

### 3.3.3 Thermal boundary resistance of the hetero-junction of Al\(_2\)O\(_3\)/graphene/Al and Al/graphene/Al\(_2\)O\(_3\) interfaces

For these two kinds of samples (the sequence indicating the layer position from top to bottom), the thickness of the Al layer is 50 nm, so the reference sample must have the same thickness as the Al layer. However, if just the reference sample is subtracted from the graphene sample, a mistake will occur. In the experiment, the graphene samples consist of two graphene interfaces and one Al/Al\(_2\)O\(_3\) interface disregarding the thermal resistance of the Al layer, on the other hand, the reference sample consists of two Al/Al\(_2\)O\(_3\) interfaces with the same consideration. Thus, one Al/Al\(_2\)O\(_3\) interface has to be added to obtain the exact thermal boundary resistance of Al\(_2\)O\(_3\)/graphene/Al (and Al/graphene/Al\(_2\)O\(_3\)) interface. To calculate the thermal boundary resistance of the Al/Al\(_2\)O\(_3\) interface, another comparison must be done between the Al\(_2\)O\(_3\)/Al/Al\(_2\)O\(_3\) sample and Al\(_2\)O\(_3\)/Al\(_2\)O\(_3\) sample.

\[
R_{th}^{Al_2O_3/Al} = R_{th}^{Graphene sample} - R_{th}^{Reference sample} + R_{th}^{Al_2O_3/Al}
\]  

(3.3)

Firstly, the thermal boundary resistance of the Al/Al\(_2\)O\(_3\) interface is measured. Fig. 3.16 shows the measurement results and it must be emphasized again that these data have a high reliability. The thermal boundary resistance is determined to be \(3.6\times10^{-8}\) K·m\(^2\)/W.

![Data plot with linear regression for the Al/Al\(_2\)O\(_3\) interface.](image-url)
After the measurement is taken, the Al sample becomes the reference sample for the graphene sample. Again, if we check the linear coefficients and the slopes, we would find the quality of the measurement to be good. The thermal conductivity of the substrate is 124 W/m·K for the graphene sample and 151 W/m·K for the reference sample. Finally, we calculated the thermal boundary resistance of the Al$_2$O$_3$/graphene/Al interfaces to be $2.8 \times 10^{-7}$ K·m$^2$/W, which should be the sum of the two separated graphene interfaces.

![Graph](image1.png)

Fig. 3.17 Data plot with linear regression for the Al$_2$O$_3$/graphene/Al interface.

There are 14 workable devices in the Al$_2$O$_3$/graphene/Al and six in the Al/graphene/Al$_2$O$_3$ sample. Fig. 3.18 summarizes the thermal boundary resistance results for these devices.

![Graph](image2.png)

Fig. 3.18 Summary of the results of workable devices.
3.4 Discussion

Before discussing the thermal boundary resistance of different kinds of interfaces, a very apparent phenomenon in this series of experiments worth discussing is the yield of the devices in the graphene samples. As stated before, all of yield rates in the graphene samples are below 40%, while the yield rates of the reference samples are almost 100%. Therefore I conclude that the adhesion of the graphene interface has an obvious influence on the stability of the whole structure. I attribute the insufficient yield of the devices in graphene samples to the weak van der Waals bonding between the graphene and the contacting substrate [39]. In EBPVD metal deposition, the upper surface of the graphene face down toward the metal target. Along with the following deposition processes on the upper surface of graphene continuing, the gravitational force on the deposited films increases. As a result, when the weak van der Waals bond cannot resists this force, the graphene interfaces begin to collapse. Usually, the transfer of graphene will introduce a non-uniform interface condition within a large area. Thus, even in the same sample, the device fabrication results are different. This is also confirmed by another result of our experiments in which a thinner layer (50 nm) of Pt is deposited on the top, the yield of the devices turns out to be nearly 100%. However, the problem of the thin Pt film samples is that the mechanical properties of such a thin layer of Pt are severely affected by the weak contacts of the graphene interfaces, as a result the Pt film cannot resist the forces from the vibration in the wire bond or the penetration in the probe press. Another clear trend in the graphene samples is that the yield of devices is better if the graphene contacts with the Al at the bottom. That can be explained by the fact that the adhesion energy is higher in the metal/graphene interface than the dielectric/graphene interface. Such adhesion energies have been measured by other researchers using the same kind of technique [40, 41]. They found the adhesion energy of the graphene/SiO$_2$ interface was around 3 J/m$^2$, while for the graphene/Cu and the graphene/Ni interfaces the adhesion energies were around 13 J/m$^2$ and 73 J/m$^2$, respectively. The variation in adhesion energy in these graphene/Cu and graphene/Ni interfaces is caused by the much stronger tendency to form covalent bonds between graphene and Ni. As graphene and Al do not tend to form covalent bonds, the adhesion energy of the graphene/Al interface is likely to have a similar value as that of the graphene/Cu interface. The adhesion energy of graphene/Al$_2$O$_3$ should be similar to that of the graphene/SiO$_2$ because both have an amorphous structure. Thus, in this study, the graphene/Al interface should have a larger adhesion energy than the graphene/Al$_2$O$_3$ interface.
In this experiment, we found the thermal boundary resistance of the Al$_2$O$_3$/graphene interface varied within a big range from $8.4 \times 10^{-8}$ to $44 \times 10^{-8}$ K·m$^2$/W. The average of the thermal boundary resistance is $27.8 \times 10^{-8}$ K·m$^2$/W, but an exact comparison with other data cannot be provided due to the limited number of devices. To explain the large variation, the two processes creating graphene interfaces need to be considered. For the transfer, before the graphene is ready to transfer to the substrates, the graphene/PMMA stack must undergo curing baking, immersion in Cu etchant and DI water. The graphene may become rippled and constrained in different degrees in different parts of the graphene due to the volume change of PMMA during curing, and the etchant and the DI water may leave residue on the surface of the graphene, making the surface of graphene become non-uniform and contaminated. The surface condition of the substrates may also vary because of the dust and other contamination. As a result of these non-uniform surface conditions in a large transfer area (1cm*1cm), the bottom graphene/Al$_2$O$_3$ interface may also become non-uniform. Furthermore, during the transfer process, micro air bubbles of or solvent may be trapped inside and due to the impermeability of graphene [23], such trapping is hard to remove.

Fig. 3.19 AFM surface scanning (10 μm*10 μm) of (a) ALD Al$_2$O$_3$, (b) (c) graphene, (d) RMS of surface roughness comparison.
Fig. 3.19 presents the surface morphology changes after graphene transfer. It confirms that for a large area, it is difficult to maintain a flat and clean interface or graphene surface. The rougher surfaces of the as-transferred samples may be caused by the contamination from both the interface and the surface. The wrinkles of the as-transferred samples may be caused by the folding or rippling of the graphene. Meanwhile, the PMMA residue is another factor causing morphology changes because an annealing process cannot guarantee 100% removal of PMMA [42].

For the second ALD deposition process, although the Al seed layer is used to promote the deposition of ALD Al$_2$O$_3$, the nucleation and growth of Al film is still non-uniform to a certain extent due to the ultralow thickness (2 nm) and the island growth mechanism of the metal film formation. The interaction at the center part of graphene crystal is different from that at the grain boundaries which provide more dangling bonds and defects [43] which are the preferred sites for the film to nucleate. In other words, this selective growth phenomenon will create a loose interface. Such factors cause the properties and structures of the interface vary with the regions. Therefore, variations in thermal boundary resistance is expected. The lowest thermal boundary resistance of 8.4*10$^{-8}$ K·m$^2$/W is at the same order of magnitude but larger than the previous 3σ measurement for the interface between SiO$_2$ and mechanical exfoliated graphene [16]. The difference have resulted from the size of the graphene flake and the sample preparation procedure. The graphene size of that measurement is about 3μm*40μm while in this case the size of the graphene sheet is 20μm*1000μm, a nearly 200 fold increase over the previous one. A larger area makes it cover more contamination into the interface. The interface contact should be more intimate in the previous measurement because mechanical press during a tape transfer method forces the graphene to adhere well to the substrates while in PMMA transfer, the operation is gentle to avoid damage to a large graphene sheet. Also the different situation of the second layer deposition may account for the different magnitude of thermal boundary resistance, but it is difficult to investigate further because of lack of information.

The thermal boundary resistance of the Al/graphene interface from different devices show a narrower range compared with the Al$_2$O$_3$/graphene interface. The average thermal boundary resistance is 7.7*10$^{-8}$ K·m$^2$/W, with a standard deviation of 2.9*10$^{-8}$ K·m$^2$/W, and the lowest thermal boundary resistance is about 3 K·m$^2$/W. All of these parameters are lower than those of the Al$_2$O$_3$/graphene interface. The stronger adhesion energy between graphene and Al, which lowers the thermal boundary resistance of the bottom graphene/Al interface
when compared with the bottom interface of the graphene/Al₂O₃ experiment, is one of the primary reasons for this reduction [44]. However, the native oxide forming on the surface of Al cannot be avoided under a conventional experiment condition. I consider the native oxide too thin to modify the properties of Al, so the interface is still treated as the graphene/Al interface. This issue can be further explained in a later discussion. Similar to the graphene/Al₂O₃ interface, the interfacial roughness and contamination also lead the thermal boundary resistance to become larger than that in the literature reports.

Another important reason for the reduction in thermal boundary resistance comes from the ease of deposition of Al onto the surface of graphene. The Al deposition does not require stronger interaction sites to nucleate, so the growth of the Al layer can cover most the surface of graphene, generating a denser and more uniform interface. These factors reduce the disorder at the interface of graphene/Al although the transfer procedure is the same as the graphene/Al₂O₃ experiment [6]. Thus, phonons can propagate more efficiently across the graphene/Al interface, resulting in a low thermal boundary resistance.

The thermal boundary resistance measurements on the hetero-junction of the graphene interfaces show that most of the thermal boundary resistance values fall into the regime of 15~30*10⁻⁸ K·m²/W. In this regime, the average thermal boundary resistance for two kinds of heterogeneous couples are 24±5.4*10⁻⁸ K·m²/W for the Al/graphene/Al₂O₃ and 25±3.4*10⁻⁸ K·m²/W for the Al₂O₃/graphene/Al. This consistency indicates that the sequence of the formation of the graphene interfaces during the sample fabrication has little influence on the thermal boundary resistance and the graphene is little changed during the different fabrication procedures. In an extreme case the actual graphene interfaces in the Al₂O₃/graphene/Al sample is the Al/graphene/Al₂O₃ because in this sample the bottom surface of graphene is in contact with the native oxide layer and the upper surface of the graphene is in contact with Al seed layer. This seems explain why there is a similar thermal boundary resistance magnitude shared by two samples actually fabricated by two different methods. However, if this assumption is true, there would be two extra Al/Al₂O₃ interfaces on the top and bottom of the Al/graphene/Al₂O₃ structure. The thermal boundary resistance of Al/Al₂O₃ interface is 3.6*10⁻⁸ K·m²/W, so the thermal boundary resistance of the Al₂O₃/graphene/Al sample should be obviously larger than the Al/graphene/Al₂O₃ sample. This also implies that my previous conclusion about the neglecting of native oxide at the bottom Al layer of the Al/graphene/Al experiment is valid. A further conclusion that can be drawn from this analysis is that the
thermal boundary resistance for the graphene interface is dictated by the region near the interface, rather than decided by the intimate materials alone, which is suggested by the fundamental review on thermal boundary resistance [1]. In a recent work on the calculation of thermal boundary resistance of the graphene/GaN interface, Hu et al found that at the interface of the strong coupling between graphene and contacting materials, the near interface zone dominates the temperature drop of the whole structure [45]. In addition, Yang et al found that at the Al/Si interface the atomic level disorder near the interface is an important aspect of interfacial phonon transport, which leads to a modification of the phonon states near the interface.

Using the average thermal boundary resistance of the Al/graphene interface to subtract these averages, I also obtain an average the thermal boundary resistance of the Al$_2$O$_3$/graphene interface of around 16*10^{-8} K-m$^2$/W, which is close to average of the smaller half in the experiment results of the Al$_2$O$_3$/graphene/Al$_2$O$_3$ sample. I regard this value as the thermal boundary resistance of a normal graphene/Al$_2$O$_3$ interface. Another phenomenon shown in Fig. 3.18 is that the ALD Al$_2$O$_3$ on top of the graphene sheet induces some anomalous high thermal boundary resistance. This is similar to the Al$_2$O$_3$/graphene/Al$_2$O$_3$ sample. Thus, the ALD Al$_2$O$_3$ deposition onto the upper surface of graphene plays a major role in causing the anomalous high thermal boundary resistance of the Al$_2$O$_3$/graphene interface. The non-uniform growth of ALD Al$_2$O$_3$ offers the near interface Al$_2$O$_3$ with a loose structure, inducing non-bulk properties at different extensions. This loose structure effect also indicates more investigation on the effect of near interface region on the thermal boundary resistance is demanded.

3.5 Conclusion

The thermal boundary resistance of large area CVD graphene interfaces is larger than that of mechanically exfoliated graphene interfaces. The large size of CVD graphene makes it easier to cover more micro contamination on the surface. The PMMA transfer technique is not able to guarantee an intimate contact interface.

The thermal boundary resistance of the Al$_2$O$_3$/graphene interface is higher than that at the Al/graphene interface. The stronger adhesion energy of the van der Waals bond between graphene and contacting materials should be responsible for the lower thermal boundary resistance. It also helps to maintain the stability of the graphene structure.
The ALD deposition of Al$_2$O$_3$ onto the surface of graphene is a major factor causing the anomalous high thermal boundary resistance because of the selective growth of Al$_2$O$_3$ at the active sites of graphene sheet i.e. grain boundaries and defects.

The near interface region affects the thermal boundary resistance of the CVD-graphene interface but it is difficult to quantify the contribution in the nominated thermal boundary resistance. A dense and orderly region near the graphene interface has a positive effect in this study.
CHAPTER 4
THERMAL BOUNDARY RESISTANCE OF
GRAPHENE/TI INTERFACE AND ANNEALING
EFFECT ON THE INTERFACE

4.1 Background

The graphene/metal interface is a very common type of interface and has attracted strong research interests in graphene applications. In graphene devices, metals are used as the electrode and put in contact with graphene to form an electrical circuit. Thus, the electrical properties of the graphene/metal interfaces have been widely investigated [46-48] and used as reasonable criteria to evaluate the quality of graphene/metal interfaces. Generally, the interaction between metals and graphene are categorized into two groups, physisorption and chemisorption. Physisorption metals, including Al, Cu, Au and Pt, form weak bonds with graphene and have little effect on the electron structure of graphene, while the chemisorption group, which includes Ti, Ni, Co and Cr, carbide bonds tend to form at the interface and significantly change the electron structure of graphene. Thus, the electrical properties of the graphene/metal interfaces can be varied by the choice of the metals in contact with graphene. It has been shown that the contacting metal can also alter the thermal boundary resistance of the graphene/metal interface [20]. As the graphene application in microelectronics aims at the realization of high frequency devices, the large amount of Joule heating will be a big issue to consider. In this situation, the metal electrode not only is responsible for conveying electrical current, but also help to dissipate heat. It has been reported that the post annealing process can not only remove the PMMA residue left by lithography process but also improve the electron mobility of graphene devices by the facilitating the formation of nickel carbide at the graphene/Ni interface [29]. The study on the thermal boundary resistance of the graphite/metal interfaces also implies that carbide formation between graphite and Ti is responsible for the smaller thermal boundary resistance when compared with that of the graphite/Al interface [18]. Therefore, it should be useful to investigate the thermal boundary resistance between graphene and the chemisorption metals interface. Recently, graphene-metal composites have become a promising research direction. Copper capped with graphene has been demonstrated to be feasible and benefits interconnect technology, this is because after being capped with graphene, the copper interconnect demo shows a reduced resistance.
and improved breakdown current density [49]. Also, the thermal issue related to the graphene/Cu interface has not been revealed yet. Another technical report shows the increasing interests in graphene-Ti composites. Researcher believe mixing graphene with Ti matrix can improve the thermal conductivity of pure Ti. Thus, the graphene/metal interface is very crucial to prove the capability of these applications. A low thermal boundary resistance can enhance the performance and the duration of such composites. In this chapter, graphene/Ti is selected FOR its thermal boundary resistance and the annealing process is introduced to tune the thermal boundary resistance.

4.2 Materials and fabrication procedure

In this study, Ti is selected to form the graphene interface. Most of the sample fabrication procedures and parameters are the same as the previous study, unless the EBPVD Al is switched to Ti by the same kind of deposition technique.

![Fig. 4.1 Structures of graphene/Ti sample (a) and reference samples (b) (c).](image)

The annealing process is carried out in a furnace. The gas environment is 95% Ar and 5% H₂ to protect the metal and graphene from oxidation. After the formation of the gas environment in the furnace, it will be heated up to 400°C and maintain for one hour. After that the furnace is allowed to cool down naturally.

4.3 Thermal boundary resistance characterization and phenomenon induced by annealing

To investigate the effects of the annealing process, thermal boundary resistance must be characterized both before and after annealing, including the reference sample. Among the three samples, I have not characterized the annealing effect on the primary reference sample which only contain an ALD Al₂O₃ layer inside, this is because the thermal conductivity of the ALD Al₂O₃ layer is believed to be stable during the annealing process [50].

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First, the Ti sample is characterized to obtain the thermal boundary resistance of the Ti/Al$_2$O$_3$ interface. Fig. 4.2 and Fig. 4.3 show a plot of the same device before and after annealing.

From these two figures, the high quality of data is again ensured. The similarity of two figures indicates that annealing process have no obvious effect on this sample. The thermal boundary resistance is determined to be $3.3 \times 10^{-8}$ K·m$^2$/W and $3.2 \times 10^{-8}$ K·m$^2$/W for the as-fabricated state and annealed state respectively.

The thermal boundary resistance of the graphene/Ti interface is characterized by the same method. The annealing process is applied on all the samples at the same time. The consistency
of the annealing is thus maintained. For calculation, the reference Ti sample of the same state is selected to use separately.

Fig. 4.4 Data plot with linear regression (as-fabricated).

Fig. 4.5 Data plot with linear regression (annealed).

Fig. 4.6 Comparison of the fitting of the as-fabricated state and annealed state.
From a comparison of these two figures, a clear decrease of the upper line which indicates the surface temperature of graphene sample is observed. There is a variation in the slopes of different states of around 10%, which is the evidence that the annealing introduced some changes to the graphene sample. The thermal boundary resistance is determined to be $3.4 \times 10^{-8}$ K·m$^2$/W and $2.9 \times 10^{-8}$ K·m$^2$/W for the as-fabricated state and annealed state respectively.

In Fig. 4.7, the thermal boundary resistance results are summarized. All the graphene samples show a downward shift in thermal boundary resistance after annealing, while the Ti samples show little change after annealing.

![Fig. 4.7 Comparison between the as-fabricated and annealed states for each device.](image)

### 4.4 Discussion

First, the thermal boundary resistance of graphene/Ti interface before annealing is discussed. The yield of devices after the whole fabrication procedure is much better than the graphene/Al$_2$O$_3$ sample, and to a certain extent it is also better than the graphene/Al sample. This phenomenon is consistent with the fact that the Ti tends to form strong covalent bonds with graphene, providing a better ability to resist collapse of the layers on top of graphene. Among the 12 devices, the results show a relative small variation thermal boundary resistance. The largest one is about 3 times the smallest. I attribute this phenomenon to the strong interaction between graphene and Ti, which leads a well adhesive interface. It is demonstrated that the Ti reacts with the ends of the graphene sheet i.e. defects and grain boundaries spontaneously with the deposition, and such interaction is not limited to ends region, which indicates that during Ti carbide formation graphene is consumed from the ends region [51].
The average of the thermal boundary resistance is $5 \times 10^{-8}$ K·m²/W, in the same order as the graphene/Al interface but the value is smaller. The thermal transport efficiency is proved to positively relate to bonding strength [10], Thus, the lower thermal boundary resistance of the graphene/Ti interface indicates their stronger interaction.

In order to investigate the effect of annealing process inducing to the graphene interface, the effect on reference structures will need to be discussed. From a comparison of Ti samples in different states, no obvious change was found. Thermal boundary resistance is similar. The derived thermal conductivity of substrate from the slope of the fitting result also gives the same result. This phenomenon indicates that the annealing process do not bring about obvious improvement or case degradation in the Ti sample. This conclusion is the baseline to investigate the annealing effect at the graphene/Ti interface. As in the graphene/Ti samples, the only difference is the insertion of graphene which creates two additional graphene/Ti interfaces when compared with Ti samples. So, the difference between the as-fabricated state and annealed state should be related to graphene. After annealing, the devices become different from the as-fabricated state. The slopes of the fitting changed. This might indicate that the thermal conductivity of the substrate changed, because slope is used to derive the thermal conductivity. But from the Ti sample experiment, the annealing has little effect on the substrate, and the change in structure above the substrate will also plays a role in the change of the slope [33]. So I think the change in slope should not be attributed to the substrate, but is due to the graphene interface. Based on this point, I still used the differential method to calculate the thermal boundary resistance in the annealed state for all the devices. The decrease happens to all the devices, the maximum is up to 50%. The majority of the devices show at least a 10% reduction in thermal boundary resistance. The average of the thermal boundary resistance is reduced to $4 \times 10^{-8}$ K·m²/W

The reasons contributing to the decrease in thermal boundary resistance are not very clear. A previous report shows the reduction in thermal boundary resistance between graphene and Au and W is a result of nonlocal laser annealing [22]. The researchers derive the thermal boundary resistance with a model used for obtaining the thermal conductivity of graphene by the micro-Raman technique. They attribute the reduction to the melting of the metal surface because of the high temperature caused by the laser. They conclude that melting transforms the interface morphology and increases the actual contact area between graphene and metal and thus reducing the thermal boundary resistance. However, in my study, the annealing temperature is far from the melting point of Ti, so it should not be the main reason for the
reduction. As the study investigating the annealing effect on the electron mobility improvement on SiO$_2$/graphene/Ni devices concludes, the formation of nickel carbide on the edge of graphene is the major reason for the mobility improvement [29]. However, the control set of SiO$_2$/graphene/Au device shows little improvement after annealing because the carbide formation is not preferred for graphene and Au. Based on this, I attribute the reduction in thermal boundary resistance to the continuous formation of Ti carbide during annealing. The adding of covalent bonding sites to graphene has been reported to be an effective way to reduce the thermal boundary resistance. The O$_2$ plasma functionalized graphene show a better thermal transport property on the graphene/metal interface, and the researchers attribute the lower thermal boundary resistance to the formation of graphene-O-metal covalent bonds [6]. However, there are still questions that remain unanswered. As the annealing process activates the formation of Ti carbide, which means the consumption of graphene continues, causing the graphene/Ti interface to become a mixture of unreacted-graphene/Ti interface and Ti carbide interface. Therefore, the side effects of formation of Ti carbide on other properties of graphene is also unknown and these side effects may cause a certain degradation to the graphene devices. Although the thermal boundary resistance is shown to have reduced by annealing in this experiment, the side effects of the annealing still remains unknown.

### 4.5 Conclusion

The thermal boundary resistance of graphene/Ti is in the same order as graphene/Al. The preferred formation of carbide between graphene and Ti makes the thermal boundary resistance smaller when compared with the graphene/Al interface which shows mostly a weak physical interaction.

Annealing process can reduce the thermal boundary resistance of graphene/Ti interface. One possible reason is that annealing assists the chemical reaction between graphene and Ti. The covalent bonds between graphene and Ti effectively help the heat transfer across the interface which is useful to enhance the thermal conductivity of graphene composites. But the side effects on other properties of graphene are not clear and this may impede the application of annealing to reduce thermal boundary resistance in graphene microelectronics application.
CHAPTER 5

SUMMARY AND FUTURE WORK

This study on the thermal boundary resistance of graphene interface demonstrate the capability of the 3ω method to characterize the thermal boundary resistance of interfaces. However, the interface adhesion impedes the application of the 3ω method on the weak contact interface. If the investigated materials are very thin, like graphene and a self-assembled monolayer, the 3ω method is an effective way to study the thermal properties.

From the thermal aspects, the thermal boundary resistance of the graphene interface plays a significant role in the nanoscale application of graphene. The weak graphene/Al₂O₃ interface will impede the heat dissipation in the graphene device integrated with Al₂O₃. A clean and dense interface of graphene/Al₂O₃ contact is desired, because it can maintain a low thermal boundary resistance. The thermal boundary resistance of graphene/Ti interface is lower than that of the graphene/Al interface, this is because the strong covalent interaction of Ti and graphene affords greater assistance to the heat transport than the van der Waals interaction between Al and graphene. The near interface region accounts for the thermal boundary resistance of interface and the mechanism is worthy further investigation. The annealing process probably enhances the Ti carbide formation between Ti and graphene resulting a reduced thermal boundary resistance of the annealed sample. However, it is also possible that the graphene is damaged thus reducing the real applications of graphene.

CVD-graphene is the best candidate to promote the use of graphene in industry, but the transfer of graphene may cause contamination and morphology change to the graphene interface, which would degrade the performance of graphene devices and graphene composites. Thus, more effort is required to develop a better transfer technique or invent a transfer free production method. Besides, it is valuable to discover some compatible and easy post-transfer process for the elimination of contamination.

Future work will focus on the characterization the mechanism of the annealing induced reduction of thermal boundary resistance. The examination of the chemical state of graphene will be conducted by the Raman, XPS and other bonding characterization techniques.

It will be interesting to investigate the thermal boundary resistance between multilayer graphene and contacting materials because the properties of graphene are thickness dependent.
to a certain degree. Furthermore, as this study focuses on the single layer graphene which is polycrystalline, a comparison between polycrystalline and single crystalline would be useful to validate the effects of defects or boundary contacts of graphene.
REFERENCE


Appendix

Matlab code for general equation to determine the temperature rise of anisotropic multilayer sample.

%Calculates the "3w profile" for N layers, each with anisotropic conductivity. The substrate (layer N) is considered semi-infinite.
%frequencies is a vector of VOLTAGE SOURCE FREQUENCIES in Hertz (NOT rad/s)
%Definitions:
%N: Number of Layers
%ky: Vector of cross-plane conductivities (layer 1 is the topmost layer, layer N is the substrate)
%kx: Vector of in-plane thermal conductivities
%Cp: Specific Heat Capacity of each layer (J/(kg*K))
%rho: Density of each layer (kg/m^3)
%d: Vector of layer thicknesses (includes substrate even if its semi-infinite)
% P: Heater power (W)
% L: Heater line length (m)
% b: Heater HALF-width (i.e. 1.5e-6 for a 3um wide line!)
%example: [deltaT,freqvect]=FullModelFunctionv4(3,[1.5 10 18],[1.5 5 18],1e7*[1 1 1],1e3*[1 2 1],1e3*[2 3 4],.5^2/30,400e-6,7.5e-6)

function [deltaT,freqvect]=FullModelFunctionv4(N,ky,kx,Cp,rho,d,P,L,b,frequencies)

kxy=kx./ky; %anisotropy
alphay=ky./(Cp.*rho); %thermal diffusivity
www=sqrt(-1); %"i"
Lfreq=length(frequencies);
freqvect=zeros(Lfreq,1);
for i=1:Lfreq
freqvect(i,1)=frequencies(i);
end

lambdamax=10*2*pi/min([d,www]);
lambdamin=0.01*2*pi/max([d,www]);
lambdainc=lambdamax/1e2;
lambda=[0,logspace(log10(10),log10(10000000000000000000000000000)),1e5]; %row vector (1 x LLambda)
LLambda=length(lambda);

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omega=2*pi*freqvect; \% column vector (LOmega x 1)
LOmega=length(omega);
omegaM=omega*ones(1,LLambda);
lambdaM=ones(LOmega,1)*lambda;
B=sqrt(kxy(N).*lambdaM.^2+www*(2.*omegaM/alphay(N)));
A=-1*ones(LOmega,LLambda);
if N~=1
for layer=N:-1:2
    Bminus=(kxy(layer-1).*lambdaM.^2+www*2.*omegaM/alphay(layer-1)).^0.5;
    phiminus=Bminus*d(layer-1);
    term1=A.*(ky(layer)*B)/(ky(layer-1)*Bminus);
    Aminus=(term1-tanh(phiminus))/(1-term1.*tanh(phiminus));
    A=Aminus;
    B=Bminus;
end
end
integrand=1./(A.*B).*sin(b*lambdaM).^2./(b.*lambdaM).^2;
integrand(:,1)=1./(A(:,1).*B(:,1));
index=1:length(lambda)-1;
integral=zeros(length(freqvect),1);
for i=index;
    integral=integral+(integrand(:,i)+integrand(:,i+1))*0.5*(lambda(i+1)-lambda(i));
end
deltaT=-P./(pi*L*ky(1))*integral;
\% END OF CODE